AN82901-1

APPLICATION NOTE

Application of Microwave GaAs FETs

9/82

INTRODUCTION

The history of converting microwave communications, as well as other communications technologies, to solid state electronics is a long one. Early advances were first made in receivers, and then in transmitters. Progress in bipolar transistor technology and the production of new semiconductor crystals during the 1960's made possible the development of such new microwave diodes as the GUNN and the IMPATT (impact avalanche and transit time). For this reason, the decade might well be called the renaissance of microwave semiconductor devices. A series of microwave communications amplifiers appeared in the first half of the 1970's which used GUNN and IMPATT diodes. They played a leading role in the trend toward solid state technology. In the middle of the same decade, a commercially feasible gallium arsenide field effect transistor (GaAs FET) appeared, and the uses of this device are still increasing. In the latter half of the 1970's, demands grew for systems more reliable than those using IMPATT and GUNN diodes. Users were demanding greater reliability, and those engaged in research and development began working toward this goal. The work is still going on today.

The demands of the industry turned the emphasis away from creating new devices to developing competition among manufacturers of semiconductors to produce devices of higher performance and greater reliability. Commercialization of GaAs field effect transistors led to lower energy consumption and smaller microwave components and systems. These are still major concerns today. With new developments in infor mation, communications and applied microwave systems, the GaAs FET has become an indispensable item.

1. THE FIELD EFFECT TRANSISTOR (FET)

In 1952, Shockley conceived the structure of the field effect type transistor and pointed out that it could be used for amplifier devices. Due to manufacturing difficulties, particularly in production technology, the field effect transistor was little known until the early 1960's. The level of technology at the time made it very difficult for people to understand the importance of the FET. But with the development of planar technology, the micro wave semiconductor industry grew with explosive rapidity.

There are three major types of FETS. The simplest of the three is the junction FET (JFET). Because of its simplicity and ease of manufacture, the JFET was the earliest to be produced commercially. It was put on the market about the same time as the first microwave bipolar transistor.

With the development of semiconductor manufacturing technology and the need for lower energy consumption, the metal oxide semiconductor FET (MOSFET) appeared. The MOSFET, like the JFET, was first developed for applications in circuits that demanded high impedance, such as input circuits in analytical instruments. Field effect transistors, particularly the MOSFET, became widely known for their use as discrete devices in UHF band communications. However, having focused solely on performance for many years, nothing in the microwave band appeared on the market which was superior to the bipolar transistor.

Around the time silicon reached its peak as a transistor material, Schottky barrier type FETs made of gallium arsenide appeared and quickly gained popularity by demonstrating their high theoretical performance. This new device, known as the Gallium Arsenide Metal Semiconductor FET (GaAs MESFET) showed performance far superior to the bipolar transistor.

This new device provided lower noise and higher gain in established solid state applications. It also provided high frequency characteristics previously unavailable from bipolar transistors. It is made by using gallium arsenide (group III-V); one of the semiconductor com pounds which has been researched continually since the latter half of the 1960's. The electron mobility of gallium arsenide is five to seven times that of silicon.

Gallium arsenide crystal technology was used to produce the GUNN, varactor and Schottky diodes, and proved to be far better than silicon in high frequency performance. A GUNN diode made of silicon would be inconceivable, so the appearance of the contemporary GaAs FET contributed greatly to developing and commercializing the GUNN diode. The reason for this is that even though the GaAs MESFET is a three terminal device, it is simple in structure and its performance depends only on the crystal quality. Advances in crystal technology have made the commercialization of FETs possible.

The GaAs FET is what is generally referred to as a "normally ON" type device. Its basic difference from the MOSFET is the use of a Schottky barrier at the gate instead of an oxide layer. This is an extremely important point. In other words, almost no GaAs FET gates are insulated from the channels in terms of direct current. Thus, even though GaAs FETs are called "normally ON" type devices, the maximum gate voltage must be zero. It does not use a dielectric like the MOSFET, so if a positive voltage is applied at the

gate, direct current flows through it. Since the gate is a very small piece of metal (0.5,μ—1.Oμ—2.0μ), the gate electrodes will fuse completely in almost all cases.

Figure 1 shows the properties of a GaAs MESFET. In almost all cases, a linear amplifier circuit biases the GaAs MESFET. This applies to other circuits as well, but considering gate bias alone, the range must be from I_{DSS}, i.e., $V_G = 0$ V, to $I_{DS} = 0$ (at pinch off, $V_G = V_P$). In this range, the voltage V_{DS} between the drain and the source has little effect on the current I_{DS} flowing through the channels. By changing the gate voltage, V_G, the drain to source (channel) current can be controlled. Figure 2 shows the transfer characteristics of a GaAs FET with n channels. This FET transfer characteristic is an important basic parameter in circuit design because it sets the bias conditions and operating point. The operating point line in Figure 2 is directly related to the mutual conductance, g_m.

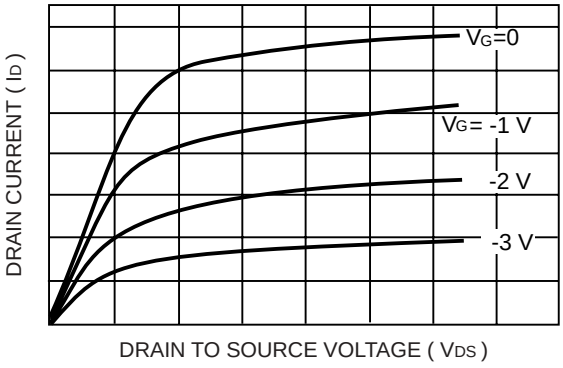


Figure 1. Typical GaAs FET DC Characteristics

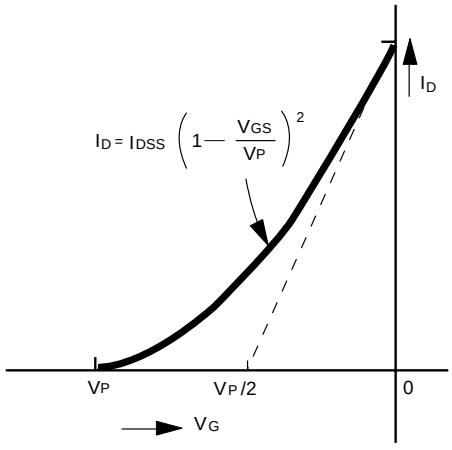


Figure 2. Square-Law Characteristic

Mutual conductance is defined as the ratio of the change in direct current to the minor change in voltage between gate sources. This is generally described as the square-law characteristic and is shown in the equation for I_D in Figure 2.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

When I_D in expression (1) is differentiated with respect to V_{GS}, the result is

$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = g_m \qquad (2)$$

and the mutual conductance for each value of V_{GS} can be obtained.

II. GaAs FET BIAS AND OPERATING POINT

The most important characteristic to consider when designing a bias circuit for small signal GaAs FETs is the previously mentioned transfer characteristic. Generally, two methods can be used to bias a GaAs FET.

1. **Dual Power Source Method**

Figure 3 shows a bias circuit which uses the dual power source method. Since the condition

$$V_P < V_{GS} < 0$$

must always apply to a GaAs FET, V_{GS} can be derived from expression (1)

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \qquad (3)$$

2. Self Bias Method (Auto-Bias)

Figure 4 shows the most universal method for reducing electrical potential between a gate and the source when there is only one power source. If the source resistance is R_S, and the operating current is I_D, then the drop in electric potential caused by R_S will be

$$I_D \; x \; R_S$$

The actual electrical potential between the gate and the source will be

$$V_{GS} = -I_D \; . \; R_S \qquad (4)$$

which is negative, so the FET can be turned on. The value R_S is obtained by combining expressions (3) and (4).

$$R_S = -\frac{V_{GS}}{I_D} = -\frac{V_P}{I_D}\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \quad (5)$$

Therefore, these are the basic bias principles.

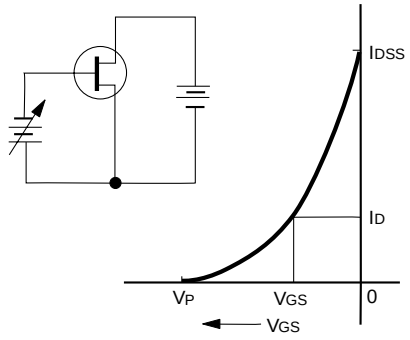


Figure 3. Dual Source Bias Method

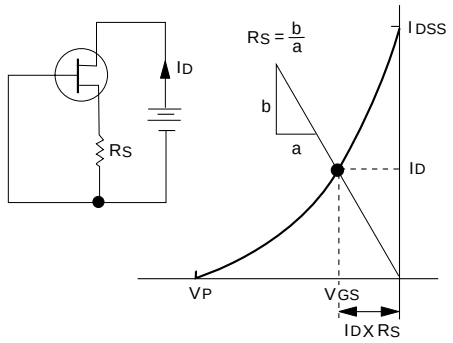


Figure 4. Self (Auto) Bias Method

Figure 5 shows the five general bias types: A, B, C, D, and E. Type A is the previously described dual power source bias method appropriate for use in the higher frequencies. When directly connecting the source to the ground terminal, source inductance can be made relatively small. By using this method, higher gain can be obtained and a lower noise factor anticipated in the higher frequencies.

All other bias methods insert a bypass capacitor into the source. Even if the high frequency performance of the bypass capacitors can be guaranteed, there will always be a loss (tan δ) resulting from the material's dielectric properties. Even with chip capacitors, there is always some inductance and care must be exercised when using them at higher frequencies. Types D and E in Figure 5 require only one power source. They are compatible with the previously described method. An advantage of this method is that if the source voltage should increase for any reason, that increase will be proportionate to the drop in potential caused by R_S, which is connected in series with the source,

$$R_S \; X \; \Delta I_D$$

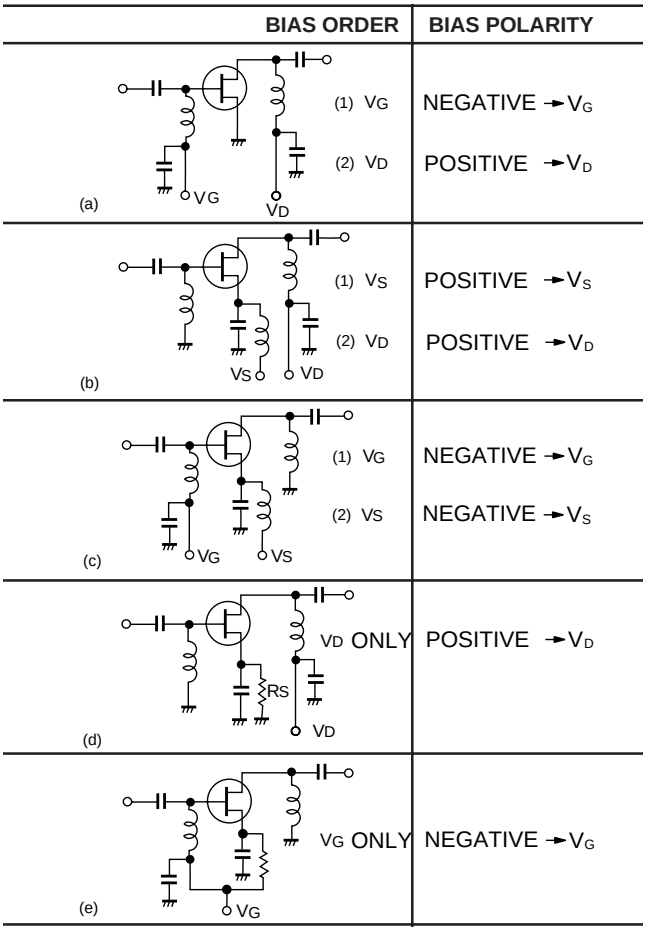


Figure 5. GaAs FET Bias Circuits

Here, ΔI_D is the increment in drain current caused by the increment in source voltage.

Drain current increase will be automatically suppressed, due to the proportionate negative bias on the gate. Generally, if a single source type (self biasing type) is selected, D is used; if the only available source is a negative one, then E should be selected.

Figure 5 shows the order for adding bias when a dual power source is used. This is to prevent, as much as possible, a

large current from flowing through the FET. The GaAs FET being discussed here generally has a high mutual conductance, giving it excellent frequency characteristics. If the gate voltage is near zero, g_m is at a maximum and oscillation may occur. For this reason, a bias scheme should be adopted that first applies a negative bias to the gate and then turns on the drain with a positive bias. There are slight differences between a bias circuit for a small signal GaAs FET and one for a power GaAs FET, but the above methods can be considered for both.

Moving one step further, let's examine a practical bias circuit. It is important to:

1. Obtain the necessary operating voltage and operating current, and
2. Ensure a high level of stability.

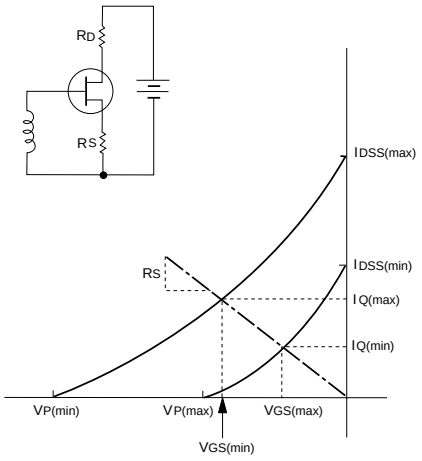


Figure 6. Possible Bias Points

Figure 6 shows the bias graph, indicating all possible bias points. Bias will be in the range determined by

$$V_{GSQ} = I_Q R_S$$

Given the bias range, the operating point for the maximum amplitude value, P, and the operating point where there is no signal, Q can be obtained. The change in I_Q from point P to point Q, or ΔI_Q, becomes

$$\Delta I_Q = I_{Q(max)} - I_{Q(min)}$$

This shows that with a variation in I_Q, the drain voltage will change only as $R_D \cdot \Delta I_Q$. If the signal midpoint is not fixed at the center of the bias line and wanders off in some direction, the wave form will be distorted. Also, the amplification operation will be degraded, and DC will flow through the gate. In a similar manner, the maximum variation in voltage between the gate and the source when there is no signal is

$$\Delta V_{GSQ} = V_{GSQ}(max) - V_{GSQ}(min)$$

I_Q is a function of both the temperature, T, and V_{GSQ}

$$I_Q = f(T, V_{GSQ})$$

If, with a variation in temperature of δT, I_Q changes by only δT_Q.

$$\delta I_Q = \frac{\partial I_Q}{\partial T} \cdot \delta T + \frac{\partial I_Q}{\partial V_{GSQ}} \cdot \delta V_{GSQ}$$

$$= \frac{\partial I_Q}{\partial T} \cdot \delta T - g_m \delta I_Q \, R_S$$

and from this

$$\delta I_Q (1 + g_m R_S) = \frac{\partial I_Q}{\partial T} \cdot \delta T$$

is obtained.

If $R_S = 0$, that is, if there is no series resistance, then

$$\frac{\partial I_Q}{\partial T} \cdot \delta T = \delta I_Q(0)$$

represents the drift. The bias stability coefficient is defined as

$$S = \frac{\textit{Fluctuation in } I_Q \textit{ with respect to Rs}}{\textit{Fluctuation in } I_Q \textit{ with independent of Rs}}$$

$$= \frac{\delta I_Q}{\delta I_Q(0)} = \frac{1}{1 + g_m R_S} \qquad (6)$$

This means that fluctuation in the entire circuit is reduced by means of negative feedback due to R_S. This effect is particularly important when using small signal FETs.

Figure 7 gives an example of a bias circuit. Since I_{DSS} and V_P often vary between devices, it is important that the bias circuit can absorb such variation, the optimum operating point can always be established, and operation is stable regardless of ambient temperatures. The circuit in Figure 7 is basically a fixed bias circuit and not a self bias circuit.

Feedback is applied to the circuit by the insertion of R_S into the source.

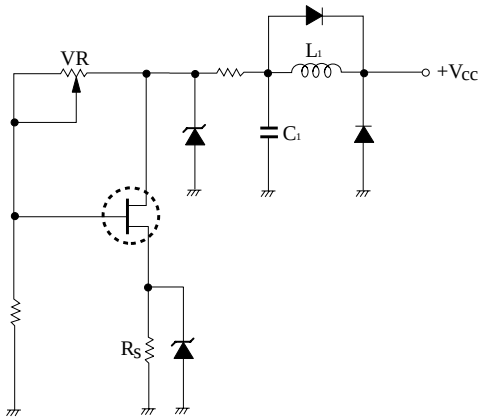


Figure 7. A Low Cost, Stable Bias Circuit

As stated previously, since the voltage between the gate and the source is $V_{GS} = -I_D R_S$ in a self bias circuit, and if I_D is known, R_S can be readily determined. In such a fixed bias circuit as the previously mentioned dual source type, the gate voltage is selected independently of R_S and I_D. Thus, it is understood that the value R_S can be higher than that when using a self-bias circuit, and the stability coefficient S can therefore be improved.

III. GaAs FET CHARACTERISTICS AND APPLICATIONS

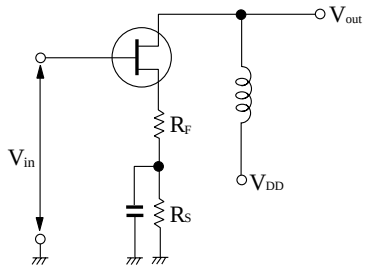
In this section, examples and explanations of GaAs FET applications will be given. The first issue is the argument as to whether or not the FET is better than the bipolar transistor because of the FET's cross modulation characteristic. Discussion will then turn to applications of the small signal FET and the large signal or power FET.

1. Distortion Factor

The transfer characteristic of a GaAs FET can be approximated using a quadratic equation, as was shown in expression (1). If the transfer characteristic could be perfectly represented by such an equation, then the second harmonic will increase to its maximum and will actually include the higher order harmonic components. To determine the value of the second harmonic for a basic frequency, substitute the total input voltage and total output current into the equation.

If there is no signal, the drain current I_D is

$$i_D = I_{DSS}\left(1 - \frac{v_{gs}}{V_p}\right)^2 \qquad (7)$$



$$KF = \frac{V}{4(V_{GSQ} - P_P)(1 + g_m R_F)}$$

$$IM = \frac{V_1 V_2}{\sqrt{2}(V_{GSQ} - V_P)(V_1^2 + V_2^2)^{1/2}(1 + g_m R_F)}$$

Figure 8. Improving the Distortion Factor Using a Series Feedback Resistance R_F

Adding a simple sine wave voltage *(Vsin wt)* to the non-signal voltage results in

$$v_{gs} = V_{GSQ} + V\sin wt$$

If the expression is rearranged and substituted into the following, then the harmonic distortion KF is

$$KF = \frac{\text{Relative value of second harmonic}}{\text{Relative value of fundamental harmonic}}$$

$$= \frac{V}{4(V_{GS} - V_P)} \qquad (8)$$

V is the maximum amplitude of the signal.
As expression (8) shows, the distortion factor approaches its minimum as V_{GSQ} approaches zero. However, as the input signal increases and enters the realm of forward gate bias, quite naturally the distortion factor increases.
Next, we will consider what happens to the cross modulation (intermodulation) produced when two sine wave signals are amplified at the same time. That is

$$V_{GS} = V_{GSQ} + V_1 \sin wt + V_2 \sin wt$$

Since the output current includes the sum and difference components of two sine waves, crossmodulation

(intermodulation) distortion, *IM*, is defined as follows:

$$IM = \frac{\text{Relative value of}}{\text{Relative value of}} \frac{\text{cross modulation component}}{\text{fundamental harmonic}} = \frac{V_1 V_2}{\sqrt{2}(V_{GSQ} - V_P)(V_1^2 + V_2^2)^{1/2}} \qquad (9)$$

Even here, we see that the distortion factor decreases as bias is brought closer to $V_{GSQ} = 0$. The main cause of the distortion is the curve (non linearity) in the transfer characteristic line, but there are other causes as well.

Distortion can also be caused by the change in output conductance, g_d, related to the operating point and the drain voltage, V_{DS}. To improve distortion, carefully select g_m and g_d, which to a certain degree work to reverse this effect.

Another point to consider is that since distortion can be produced internally, *KF* and *IM* can both be improved by applying feedback to the circuit.

As shown in Figure 8, by adding a resistance, R_F, in series with the source resistance, the distortion factor for the non-bypass feedback is calculated, using expressions (10) and (11).

$$KF = \frac{V}{4(V_{GSQ} - V_P)(1 + g_m R_F)} \qquad (10)$$

$$IM = \frac{V_1 V_2}{\sqrt{2}(V_{GSQ} - V_P)(V_1^2 + V_2^2)^{1/2}(1 + g_m R_F)} \qquad (11)$$

By applying feedback to the circuit, both the distortion factor and the bandwidth can be improved. The value of R_F will reduce the total gain only by its relative portion. It is possible to have a wide-band amplifier with a low distortion factor by initially designing the amplifier for high gain and tuning the gain to its optimum level by using feedback.

2. Small Signal FET Applications

The first practical and commercially available GaAs FET was introduced around 1973. Since then, many small signal amplifying devices with 1µm gate lengths and smaller have been marketed.

The greatest advantages for these devices are found in the higher frequency bands. Compared to the silicon bipolar transistors and tunnel diodes, GaAs FETs are far better in terms of noise, gain and output-power saturation characteristics. Other than their primary use in ultra-high frequency amplifiers, such as those for electronic countermeasures (ECM), most small signal FET applications are in low-noise amplifiers. They are used in both line-of-sight and over-the-horizon microwave communications, and in earth stations communicating with satellites.

A low noise amplifier is designed by minimizing the noise measure, *M*, shown in expression (12).

$$M + 1 = 1 + \frac{NF - 1}{1 - (1/G)} \qquad (12)$$

NF is the amplifier noise factor.

G is the amplifier gain.

In single-stage amplifiers, the general procedure for matching input circuits is to mimimize the noise factor, NF; for matching output circuits, the gain is maximized.

From observations of the input-output impedances of a GaAs FET, it is noted that there is generally a difference in impedance between maximum gain and minimum NF. This difference is particularly apparent at lower frequencies. As the frequencies go higher, the difference seems to decrease. The noise factor, which is a function of device gain, will be low when the gain is maximized at high frequencies. However, of the commercially available GaAs FETs having characteristics which allow a gain of 8 to 10 dB or more, there is still a difference between the impedance at maximum gain and the impedance at miminum NF. This difference will be seen until the frequency range approaches the X band.

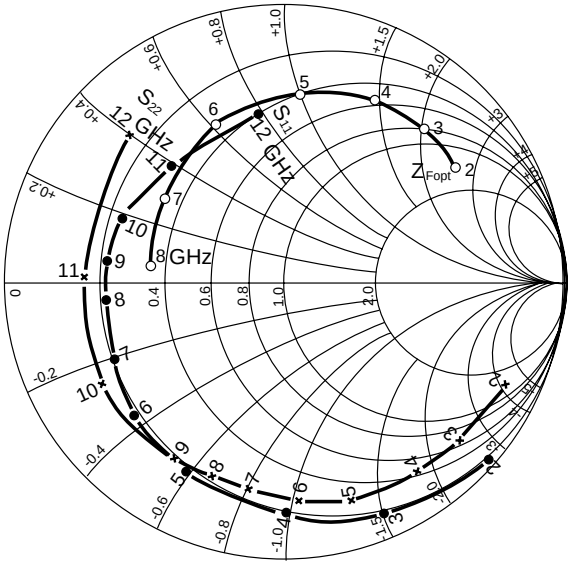


Figure 9. Frequency Characteristics Of S_{11}, S_{22}, and Z_{Fopt} in the NE24406

Figure 9 shows S_{11} and S_{22}, indicating input output impedance for the NE24406 and the signal source impedance when the noise factor, NF, is minimized. Circuits can be matched using these impedances. As mentioned previously, input circuit matching is accomplished by matching to Z_{Fopt}; and output circuit matching is accomplished by matching to S_{22}.

In the design of a multi-stage amplifier, the first and second stages are designed so that *(M + 1)* will be minimized, and the third and subsequent stages are made in such a way that their gain is maximized. Or, alternately, the amplifier can be designed according to the characteristics determined by the frequency and the device.

One impedance matching circuit, shown in Figure 10(a), is the well known Tchebycheff filter type multi-stage impedance matching circuit. The distinctive feature of this circuit lies in its applicability to the input/output circuits of wideband amplifiers. In many cases, the circuit is used in amplifiers covering the band range 8 GHz to 12 GHz and above. Although this type of matching network was originally applied to comparatively narrow bands (such as a 500 MHz bandwidth at 4 GHz), the matching circuits shown in Figure 10(b) and (c) are now believed to be best suited for bands having approximately a 10 to 15 percent ratio to the amplifier's center frequency.

For these bandwidths, the NF can be reduced to its lowest absolute value. If the widest possible bandwidth is the objective, then reduction of the NF to its absolute minimum is not possible throughout the band. In the former amplifier, the most important consideration is reducing, as much as possible, the loss in the impedance matching circuit. The Tchebycheff filter type impedance matching circuit in Figure 10(a) uses a large number of components and is not well suited for obtaining a low loss matching network.

As Figure 9 shows, both S_{11} and S_{22} go from capacitive to inductive with increasing frequencies. Consequently, S_{11} and S_{22} can use the circuit in Figure 10(b) for frequencies which exhibit a capacitive response, or the circuit of Figure 10(c) for the frequencies which exhibit an inductive response. In Figure 10(b), for frequencies slightly higher than the amplifier's center frequency, the GaAs FET input or output has a resonance of either L_1 or L_2 (with a reactance of 0), which is then matched to the desired impedance by the λ/4 impedance conversion circuit. This is only one of the countless possible impedance matching circuits. However, this is a very effective design method for low noise amplifiers requiring a band ratio of 10 to 15 percent when the amplifier's center frequency is 4 GHz or greater.

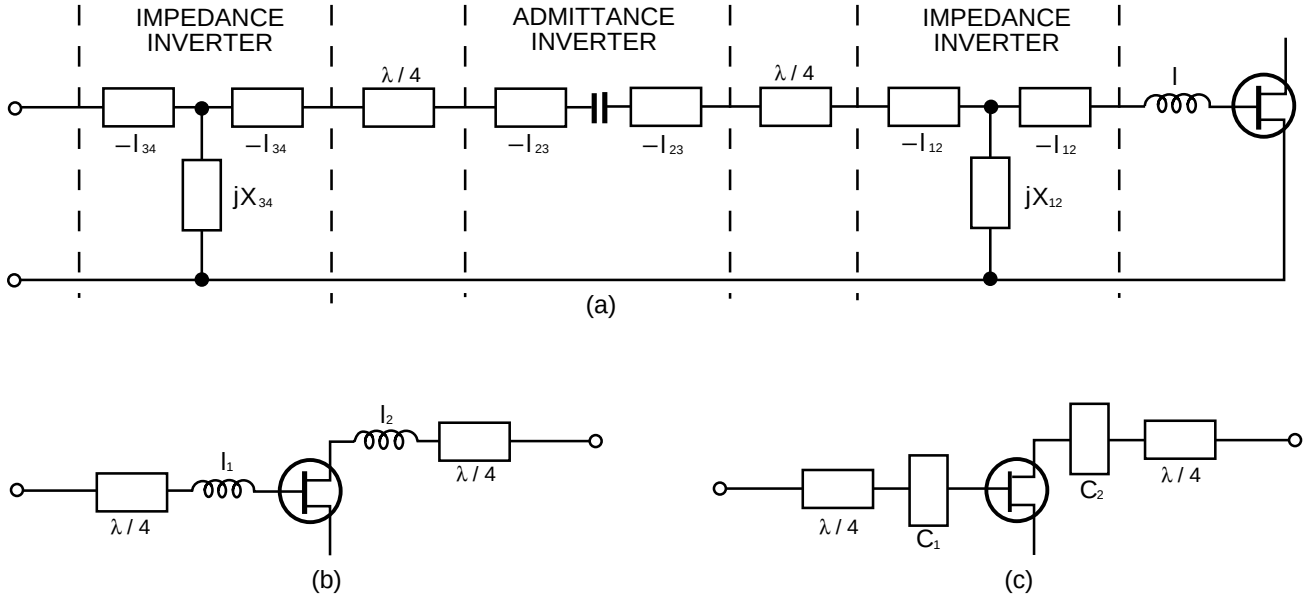
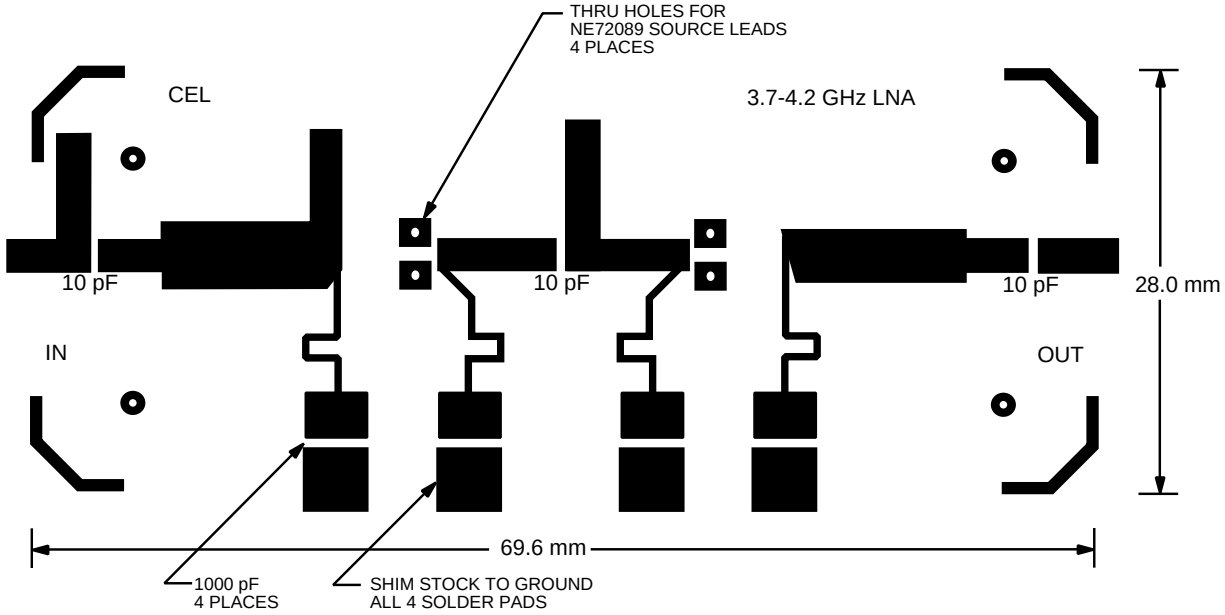


Figure 10. GaAs FET Matching Networks

3. Low Noise Amplifiers in the 4 GHz Band

Figure 11 is an example of a two-stage low-noise amplifier for the 3.7 to 4.2 GHz band using either the NE21889 or the NE72089. The matching circuit in Figure 11 is based on the same idea as Figure 10(b). It uses a microstrip with an 0.8 mm thickness teflon glass fiber substrate and transistor leads with lumped constant inductance. Figure 12 shows the schematics. Figure 13 shows the gain and noise factor normally obtained using this circuit.



Parts List: NE72089 FET (2 ea.) California Eastern Laboratories
10 pF Chip Capacitors (3 ea.) ATC #100A-100-J-P-X-50 or equivalent
1000 pF Chip Capacitors (4 ea.) Johanson #50R11W102KP or equivalent
1500 pF Feed-through Capacitors (4 ea.) Erie #2425-003-W5U0153AA or equivalent
Ferrite Beads (4 ea.) Fairrite #2643001301 or equivalent

Figure 11. PCB Layout of a 2-Stage Amplifier in the 3.7 GHz-4.2 GHz Band

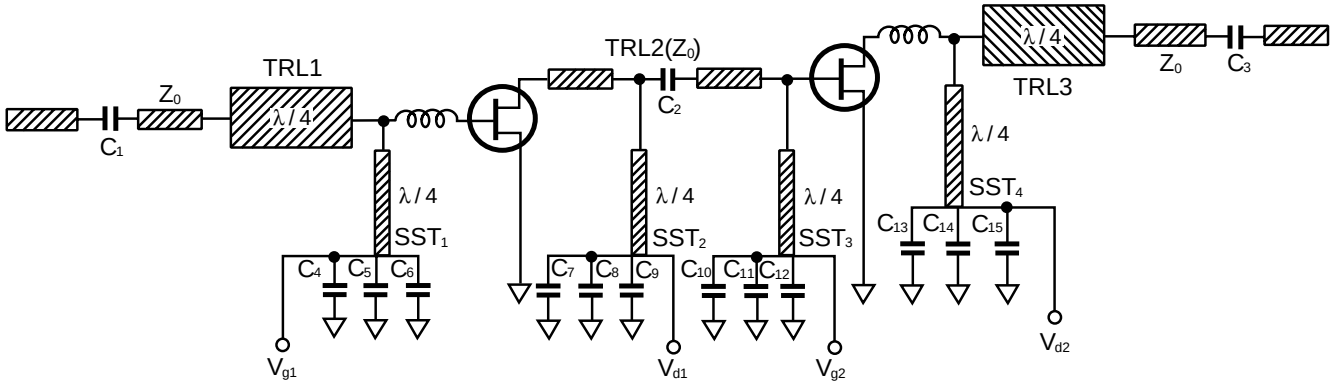


Figure 12. Schematics for a 3.7 GHz-4.2 GHz Band 2- Stage Amplifier

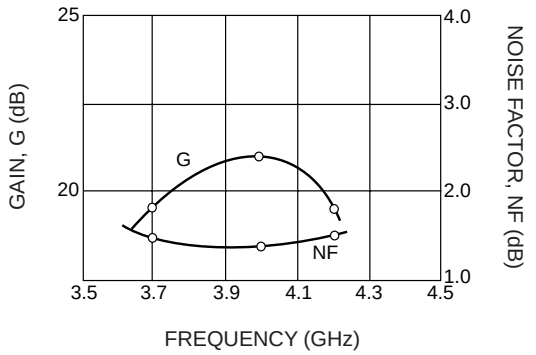
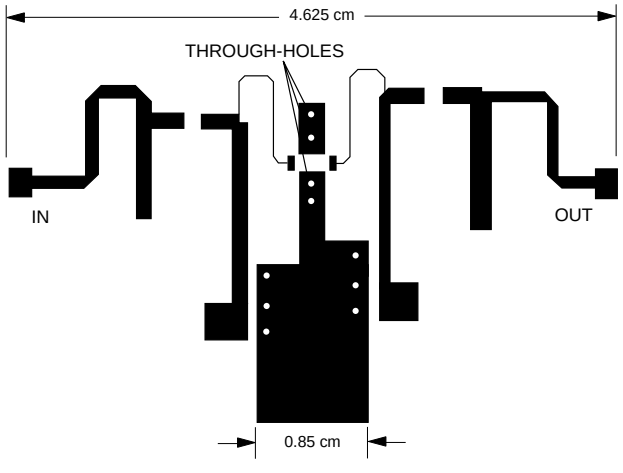


Figure 13. Frequency Characteristic of NF and G for the NE72089 2-Stage Amplifier

This two-stage amplifier uses the inductance in the first stage input section to produce resonance. Then, using the λ/4 impedance transformer, it forms a matching circuit for the 50Ω characteristic impedance. Since there is a relatively small difference in values between $S_{11}$and S_{22}, the intermediate stage matches impedance by the simple means of a transmission line.

Output matching is done in the same way as in the first step, i.e., the matching circuit shown in Figure 10(b) is used. Figure 11 is a full-scale pattern showing lines and open stubs inserted in parallel. Although these are not necessary for the ideal design, they are included to correct impedance matching problems caused by the printed circuit board connectors (microstrip to coaxial connection) and the DC blocking chip capacitors. They are inserted after the design is completed.



MATERIAL 0.8 mm THICK TEFLON GLASS

Figure 14. PCB Layout for 1.0-1.4 GHz Amplifier

4. Low Noise Amplifiers in the 1 GHz Band

Figure 14 shows a PCB layout for an amplifier designed for low noise operation in the 1 to 1.4 GHz band. Since the microstrip lines used are very thin, the diagram shown here is twice the actual size. During the design, it should be drawn four times the actual size and then reduced.

Figure 15 shows the equivalent circuit. In the design of this circuit, a band ratio of 10 to 15 percent was not obtained as with the previous amplifier. Instead, emphasis has shifted to making the band as wide as possible and the noise factor as low as possible. Since it is in the relatively low-frequency 1 GHz band, the loss due to the reactance elements (including the microstrip) was not given much concern. The Tchebycheff filter type multi-stage impedance matching circuit could have been used. However, considering the frequencies involved and the large physical size of such a circuit, a method was chosen that gives the transmission line as high an impedance as possible for input and output, and which would gradually match to the characteristics impedance of 50Ω. Figure 16 shows the typical performance characteristics of this amplifer.

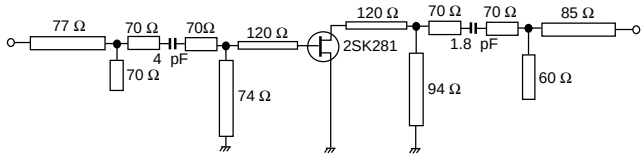


Figure 15. Equivalent Circuit for a NE72089 Low-Noise Amplifier

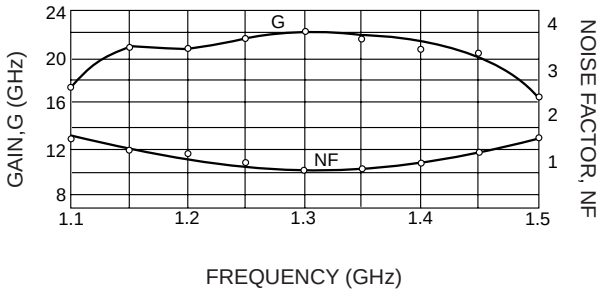


Figure 16. NE72089 Low-Noise Amplifier

When this amplifier was designed, a 4 pF blocking chip capacitor was used as part of the matching circuit, as shown in Figure 15. The input matching circuit was designed chiefly

to obtain matching for the noise factor. The data used for the NE72089 is shown below:

f	Γ_{Fopt*}	F_{min}	G	NF @ 50 Ω
1 GHz	0.59<32.5	0.6dB	17.5 dB	1.73 dB
1.3 GHz	0.65<47.0	0.6 dB	15.0 dB	1.74 dB

V_{DS} = 3 V, I_{DS} = 10 mA

*(Γ'_{Fopt} signifies the reflection coefficient obtained when comparing the signal course impedance with 50 Ω when NF is minimized)

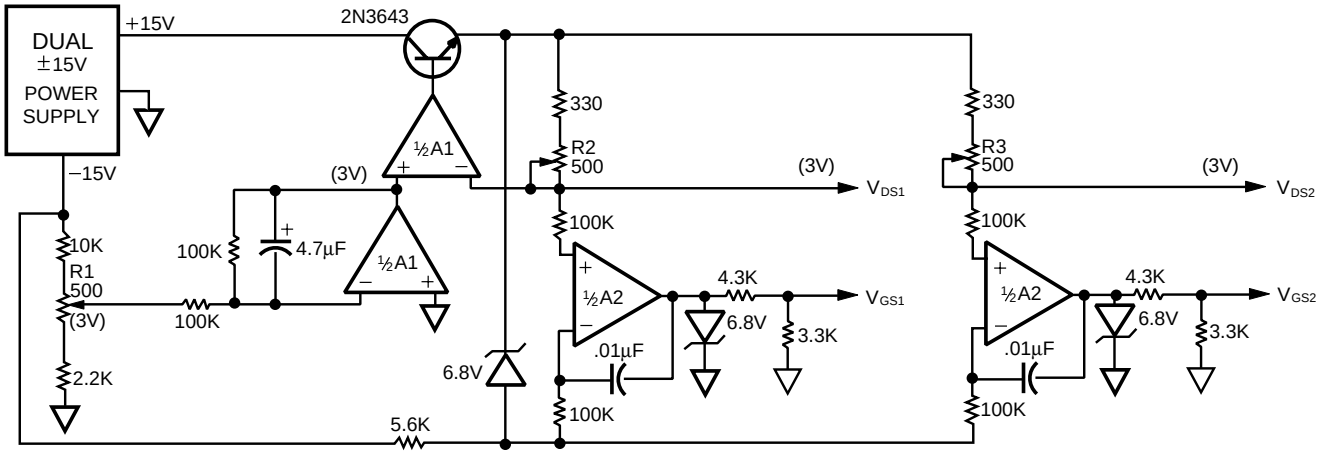
The bias circuit used to actuate this amplifier is shown in Figure 17. The figure shows a bias circuit for a two-stage amplifier. For a single stage amplifier, only one half of the redundant portion of the circuit would be used. This circuit is a constant voltage, constant current type bias circuit, one of the most applicable examples of circuits for use in small-signal amplifiers.

5. Applications to Other Amplifiers

(A) A technique of attaining wide band performance by inserting a source inductance.

L. Neven, et al., have proposed a type of feed back circuit for relatively low frequency GaAs FET amplifiers. For amplifiers operating in the 1 GHz to 2 GHz range, these circuits guarantee a low noise factor as well as good input-output impedance.

Figure 18 shows what is considered the universal GaAs FET equivalent circuit. In this circuit, drain noise current, I_{dn}, is referred to the input by the Vander-Ziel theory, then the gate source resistances, R_i, becomes noiseless and, R_S remains noisy. The noise currents at the gate and drain have been removed from the two-port. The circuit in Figure 18 is better handled by computers, where the noise and signal are compared as a function of the externally added source inductance. In this instance, it is easier to consider the equivalent circuit shown in Figure 19.



A1 AND A2: 747 DUAL OP-AMP
ALL RESISTORS: 1/4 Watt

Figure 17. Two Stage GaAs FET LNA Bias Supply

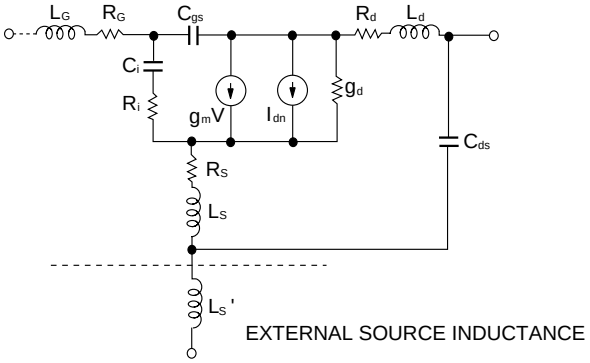


Figure 18. Universal GaAs FET Equivalent Circuit

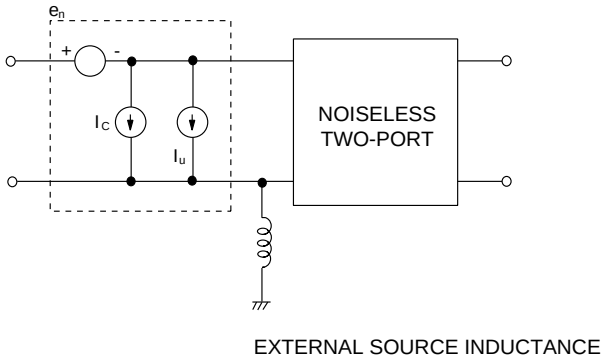
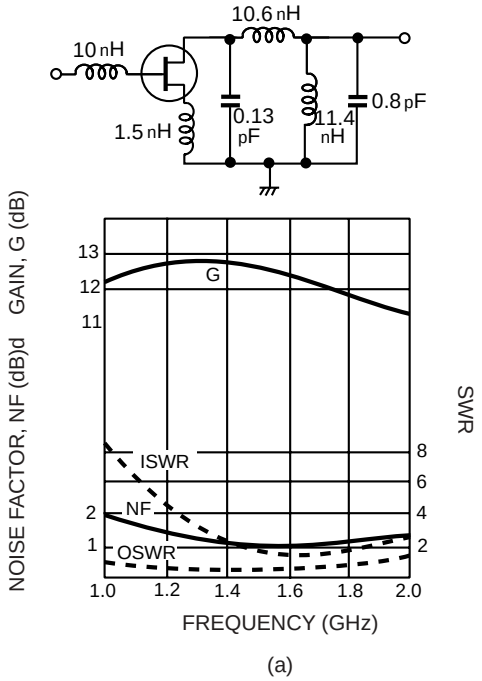


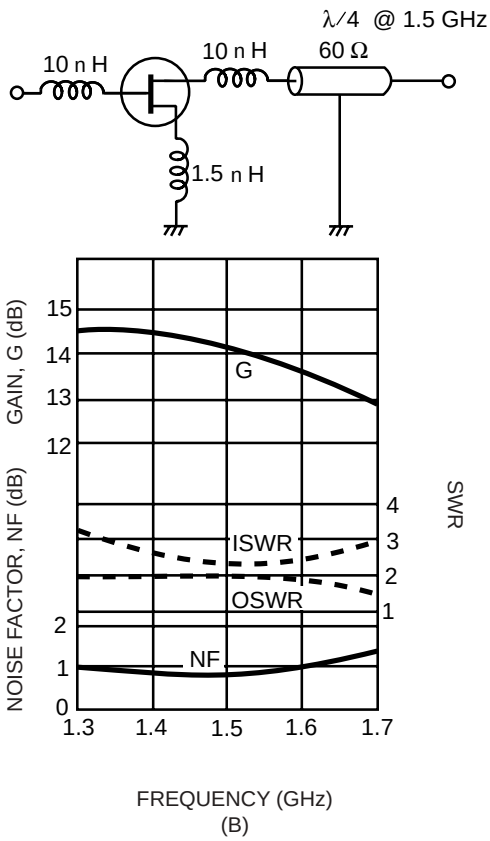
Figure 19. Cascade Connection of Device's Noise and S-Parameter Circuits

Figure 19 shows the cascade connections of the device's noise and S-parameter equivalent circuits. The circuit should be designed so that matching is obtained for the input-output impedance given to this equivalent circuit. After the design goals have been chosen, the noise figure, NF, and impedance matching networks are calculated. The circuits and characteristics of an amplifier designed by this method are shown in Figures 20(a) and 20(b).



(a)

Figure 20(a). Lumped Element Matching Network



(B)

Figure 20(b). Transmission Line Matching Network

(B) Ultra-wide band amplifiers using GaAs FETs.

The method normally used to achieve wide-band amplification involves applying negative feed back to the transistor. This method improves the VSWR and dynamic range characteristics and also ensures very flat gain response. Another method for achieving wide-band amplification involves using a balanced amplifier design which ensures good VSWR. This method is widely used in applications that cover frequency ranges of one to several octaves in the higher frequency bands. However, it is difficult to obtain a very wide band using a 3 dB, 90° coupler while also trying to ensure good input-output VSWR in ranges exceeding 10 octaves, or in the low frequency ranges. Figure 21 shows an equivalent circuit for the balanced amp.

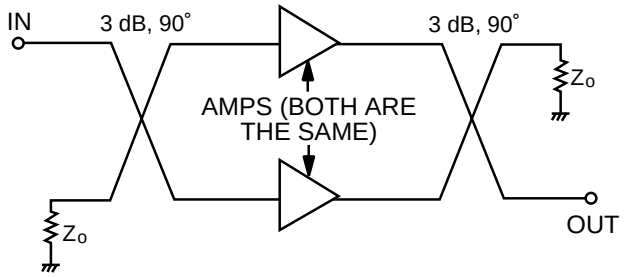


Figure 21. Balanced Amplifier Allowing Wide-Band Amplification

The use of GaAs FETs with negative feedback is an effective method of ensuring low cost and simplicity for bandwidths exceeding 10 octaves.

Figure 22 shows the basic circuit for negative feedback amplifiers. For the sake of simplicity, the DC bias circuit and the coupling capacitors have been omitted. If the characteristics of the GaAs FET to be used are suitable at frequencies of 10 MHz to 2 GHz, the device's parasitic elements will be small in size, and the equivalent circuit can be simplified to that shown in Figure 23. The simplified equivalent circuit shown in Figure 24 is obtained by adding the negative feedback resistor shown in Figure 22 to the circuit in Figure 23. The S-parameters may now be calculated for this situation.

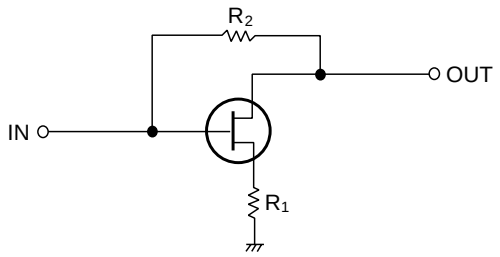


Figure 22. Basic Feedback Amplifier Circuit

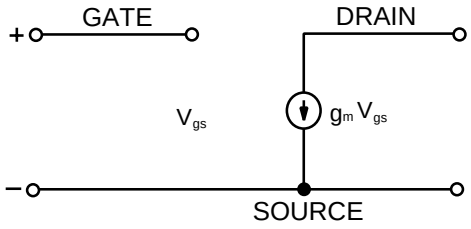


Figure 23. Equivalent Circuit for GaAs at Low Frequency

The admittance matrix can be determined by using the following expression.

$$\begin{bmatrix} I1 \\ I2 \end{bmatrix} = \begin{bmatrix} \frac{1}{R2} & -\frac{1}{R2} \\ \frac{gm}{1+gmR1} - \frac{1}{R2} & \frac{1}{R2} \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix} \quad (13)$$

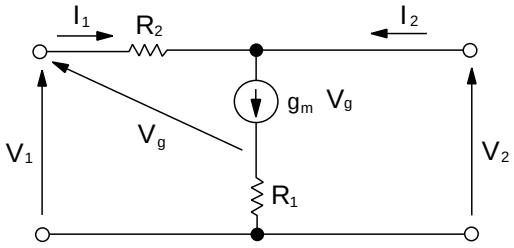


Figure 24. Simplified Feedback Amplifier Equivalent Circuit

If at this time, the input-output for Figure 24 is terminated at Z_0, the S matrix can be easily obtained by using expression (13).

$$S_{11} = \frac{1}{\Delta}\left[1 - \frac{g_m Z_0^2}{R_2(1+g_m R_1)}\right] \quad (14)$$

$$S_{22} = \frac{1}{\Delta}\left[1 - \frac{g_m Z_0^2}{R_2(1+g_m R_1)}\right] \quad (15)$$

$$S_{12} = \frac{1}{\Delta}\left[\frac{2Z_0}{R2}\right] \quad (16)$$

$$S_{21} = \frac{1}{\Delta}\left[\frac{-2g_m Z_0}{1+g_m R_1} + \frac{2R_0}{R_2}\right] \quad (17)$$

$$\Delta = 1 + \frac{2Z_0}{R_2} + \frac{g_m Z_0^2}{R_2(1+g_m R_1)}$$

Assuming that a negative feedback amplifier must improve VSWR, the input and output reflection coefficient must be 0, then expressions (14) and (15) become

$$S_{11} = S_{22} = 0$$

From this, the following expression can be derived:

$$1 + = g_m R1 = \frac{g_m Z_0^2}{R_2} \quad (18)$$

When expression (18) is substituted into expressions (16) and (17), the following results are obtained

$$S_{21} = \frac{Z_0 - R_2}{Z_0} \quad (19)$$

$$S_{12} = \frac{Z_0}{R_2 + Z_0} \quad (20)$$

Then, using expression (18), R_1 is obtained as follows

$$R_1 = \frac{Z_0^2}{R_2} - \frac{1}{g_m} \quad (21)$$

Since the transconductance, g_m, in a GaAs FET is not usually large enough, the equation $S_{11} = S_{22} = 0$ will not be satisfied. However, the range of the g_m values needed to satisfy the expression can be calculated. If $R_1 = 0$ then

$$S_{21} = I - g_m Z_o \quad (22)$$

is obtained, and thus

$$g_m|\ min = \frac{1 - S_{21}}{Z_o} \qquad (23)$$

For example, consider the design of an amplifier with 10 dB gain. Logically, if we take the input output VSWR as a low value and the characteristic impedance, Z_0, as 50Ω, when $S_{11} = S_{22} = 0$, then substituting this in expression (23) yields,

$$\frac{1 - (-3.16)}{50} = 0.082\ S$$

It will therefore be acceptable if g_m⊕83mS. Figure 25 shows the characteristics of an ultra wide band amplifier designed using this method.

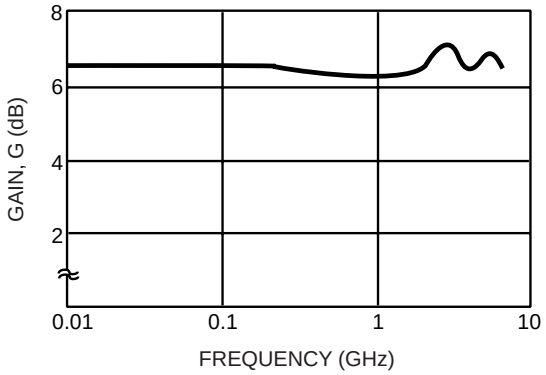


Figure 25. GaAs FET Feedback Amplifier

6. Relation of Ambient Temperature, Frequency and Noise Temperature in GaAs FETs

Up to this point, only the applications of GaAs FETs in amplifiers have been examined. Now, the discussion will turn to the relationship between ambient temperature and noise temperature.

Noise in a GaAs FET is chiefly thermal noise. Since there is rarely shot noise, the noise temperature in an amplifier changes greatly in response to the ambient temperature. Figure 26 shows the relationship of operating temperature and the noise temperature for the NE67383/NE71083. The noise temperature, T_e and ambient operating temperature, T_a, can be shown to correspond to the following:

$$Te = K \frac{\omega Cgs}{g_m} T_A \qquad (24)$$

Figure 26 shows the linearity in the relationship between the ambient operating temperature and the noise temperature. By taking advantage of this characteristic, a super low-noise amplifier can be produced by cooling the amplifier with carbonic gas, liquid nitrogen or liquid helium.

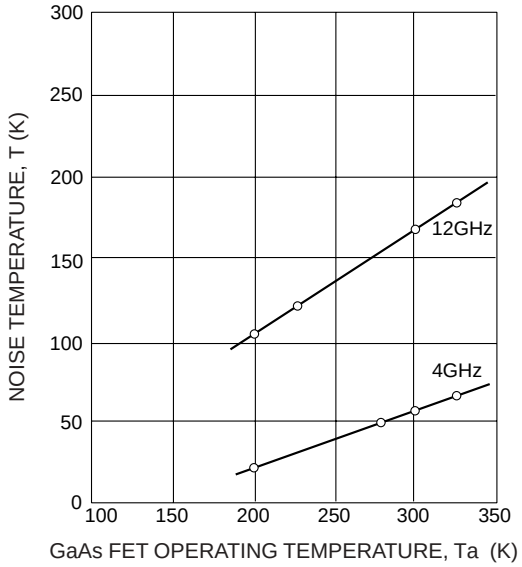


Figure 26. T_e vs. T_a for the NE67383/NE71083

7. Power GaAs FET Applications

For the small signal GaAs FETs discussed so far, we have covered only those signal levels in the range in which operating characteristics are not dependent on signal voltage or signal current. In other words, each terminal's voltage and current was in a range which satisfied a linear relationship. As the signal level increases, this relation- ship is no longer satisfied and we have a situation known as large signal operation. Of course, even if the element is in non-linear operation, the electrophysical quantity of the signal frequency is still in a linear relationship if non-linearity is small. Thus, the S-parameter relationship in a GaAs FET can be determined for small signal operation.

Because the voltage and current-to-terminal conditions which define each parameter are not fixed for large signal operation, it is difficult to determine parameters indicating a linear relationship.

Figure 27 is a simplified diagram showing the small and large signal operation of a Class A GaAs FET. Load lines A and B indicate the optimum conditions for maximum input and output when the input gate signal voltage is V_{GA} and V_{GB}.

The optimum load for small signal operation is equal to the drain conductance $(\partial I_{DS}/\partial V_D)$. In large signal operation, however, the input signal level will increase and gate voltage, V_G, will enter the nonlinear zone. The output current, which is the drain current, I_D, will then reach its upper limit and the load line gradient must increase to increase the output power. Therefore, when designing a circuit, it is necessary to use data which takes all factors into consideration.

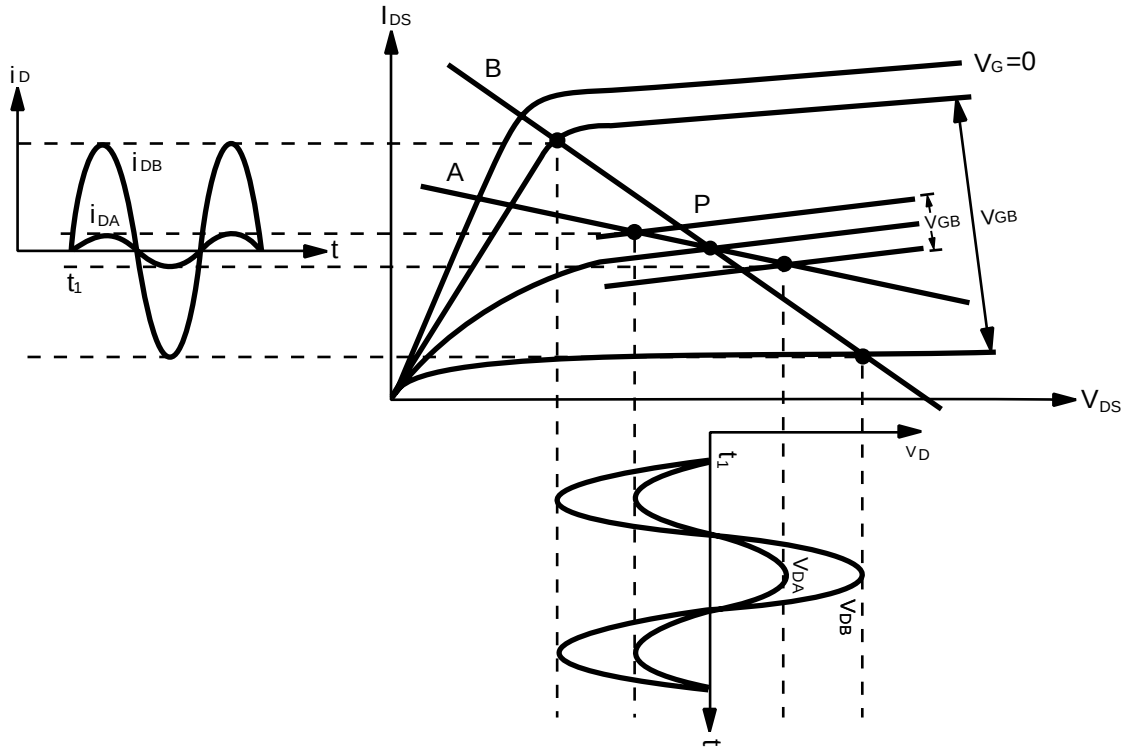


Figure 27. Simplified Load Line for a Class A GaAs FET in Small and Large Signal Operation

8. Operating Methods for Power GaAs FETs

(A) Introduction

An important factor to consider when working with Power GaAs FETs is power GaAs FETs are basically a group of small signal GaAs FETs connected in parallel so that they can handle a large power source. Therefore, they have an extremely high transconductance. Another important and necessary factor to consider is at which bias point operation takes place. Consideration must be given as to whether there is adequate bias resistance to suppress the gate current. As mentioned previously, Schottky gates are used in a GaAs FET, and there is the possibility that the operating point will cause an excessive current to flow across the gate.

The gate structure in a GaAs FET is very delicate, with a typical gate length of 0.5/μm to 1.0μm. In some cases, just a slight current flow across the gate will have a current density of 10^6A/cm^2. With such high current density, the gate will eventually fail.

Figure 28 shows the change in input-output characteristics due to the increasing gate current. Here, the operating drain voltage is constant, but direct current begins to flow in the opposite direction at the gate when the input signal level is increased sufficiently. When the input signal power increases, the Schottky gate is biased in the forward direction and gate current begins to flow in that direction. Caution must be taken at this time since the amount of gate current has a bearing on whether or not the FET will be destroyed.

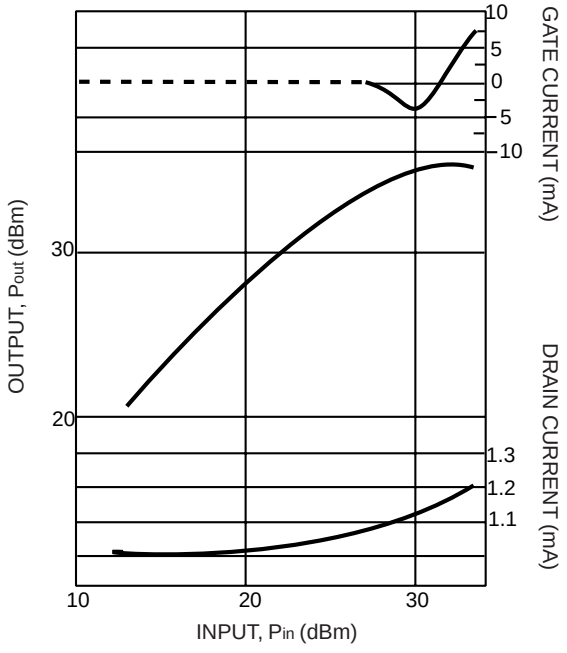


Figure 28. Relationship of Input-Output Characteristics to Increasing Gate Current

(B) Bias Circuits

Table 1 shows the maximum allowable gate current for each of NEC's high power GaAs FETS. Care should be taken at all times when planning bias circuits and input power to ensure that these values are not exceeded.

NE8001	3.0 mA
NE8002	6.0 mA
NE8004	10.0 mA
NE8008	15.0 mA
NE3716	20.0 mA
NE9000	0.5 mA
NE9001	1.3 mA
NE9002	2.6 mA
NE9004	5.0 mA
NE9008	8.0 mA
NE8681	3.0 mA
NE8682	6.0 mA
NE8684	10.0 mA
NE8688	15.0 mA
NE8691	1.3 mA
NE8692	2.6 mA
NE8694	5.0 mA

Table 1: Maximum Allowable Gate Currents for the NEC Power GaAs FET Series

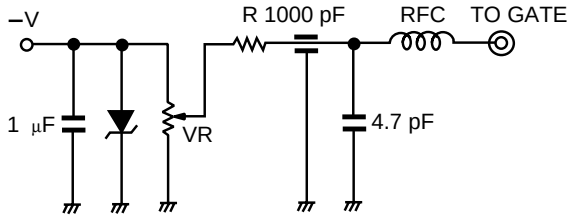


Figure 29. Example of a Gate Bias Circuit

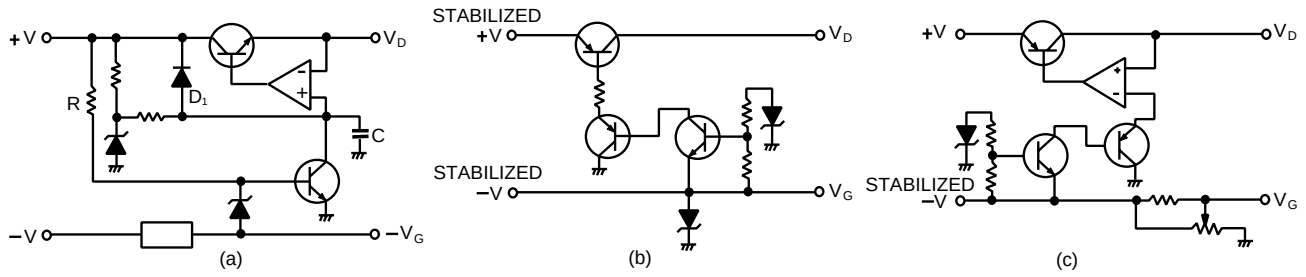


Figure 30. Power GaAs FET Bias Circuits

One thing that is very basic when biasing power GaAs FETs is the need for increased impedance of the gate bias circuit. The example in Figure 29 shows a type of feedback circuit incorporating a resistor in series with the bias circuit which produces a drop in potential when the current across the gate begins to increase, and adds to the gate series bias. By inserting a low pass filter, such as an RFC or capacitor, unnecessary oscillation or phase shift will be prevented.

Another important factor is the order in which bias is applied. It is generally disadvantageous, both thermally and electrically, to self-bias a power GaAs FET. Therefore, a positive and negative dual power source should be used to bias the drain and gate separately. For a GaAs FET, maximum current will flow when the gate voltage is at zero. With a high output level FET, I_{DSS} is sometimes greater than several amps and since typical g_m is extremely high, oscillation will occur and the FET will be destroyed either thermally or electrically. For this reason, any appreciable flow of high current must be prevented from reaching the drain. The bias method used must be one whereby negative voltage is applied to the gate first, after which positive voltage is applied to the drain. The following is a detailed example of this method.

(1) Add a negative potential to the gate which is close to -5V or to the pinch off voltage.

(2) Specify the drain voltage in such a way that it moves as rapidly and smoothly as possible from zero volts to the preset V_D. If there is no possibility of a surge voltage being produced and the drain voltage is completely stable, add the preset voltage instantaneously.

Figure 30 gives three recommended bias circuits for biasing power FETS. Figure 30(a) is an excellent bias circuit because there are no limitations requiring that either positive or negative voltage be applied to the circuit first. Drain voltage, V_D, will reach its preset value according to the time

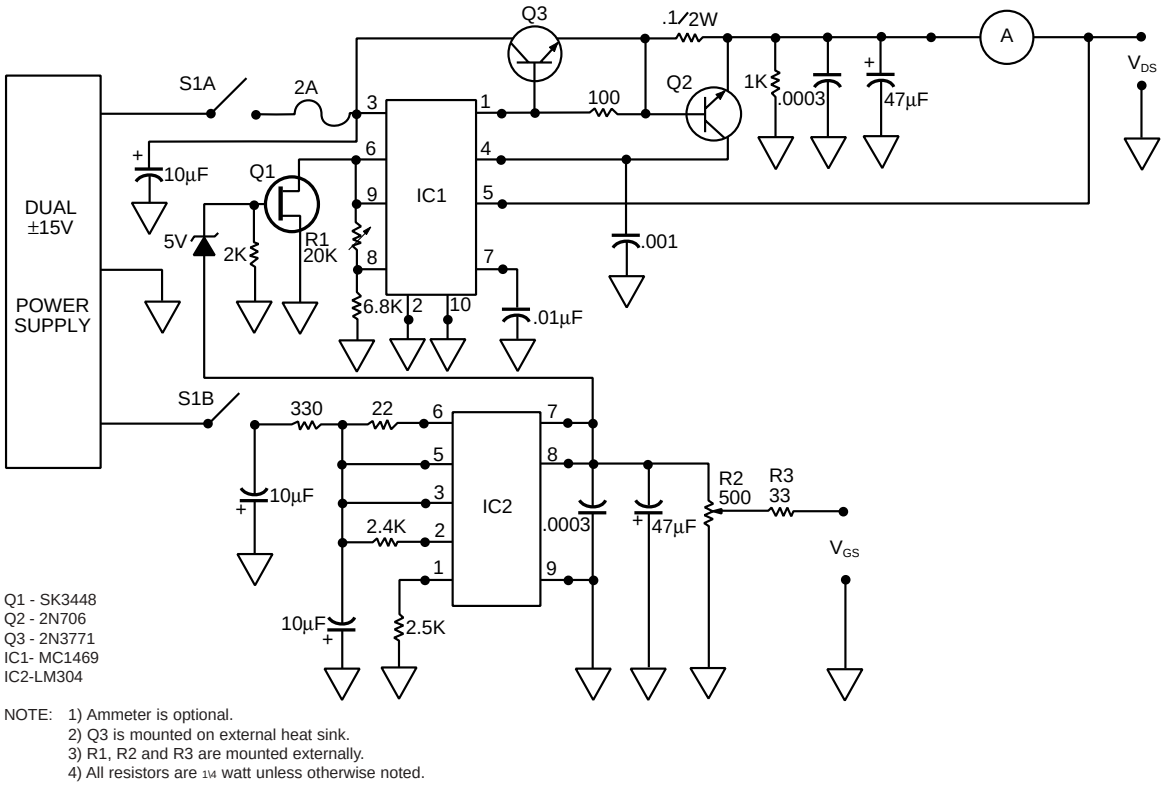


Figure 31. Power GaAs FET Regulated Bias Supply

constant determined by *C* and *R*. When the power source is OFF, the electrical charge will pass through diode D_1, and return quickly to the power source side, thus the FET can then be safely biased.

Figure 31 shows a bias circuit recommended for biasing a multistage (5 stages) power GaAs FET amplifier.

9. Examples of C-Band Application Circuits Using NEC's Power GaAs FET Series

With the exception of the devices with the 96 package, NEC's C-Band GaAs FET series using multiple chips contain internal matching network (IMN) circuits within the packages. The IMNs are not intended to match the devices to 50Ω but to facilitate and reduce the external matching networks. The GaAs FET series which are in 98 packages have both input and output matching circuits close to VSWR, 1:2.5. The devices in 95 and 98 packages which have internal matching circuits are identified by the numbers -4, -5, (-5H), -6, -7, (-7H), and -8. Each of these numbers indicates the center frequency at which the IMN circuit is optimized and tested. For example, -4 is at 4 GHz (3.5-4.5 GHz) and -6 is at 6 GHz (5.5-6.5 GHz).

Figures 32 to 68 relate typical characteristics and illustrate application circuits using an 0.8mm thick teflon glass circuit board. The units used in these charts are millimeters (mm). Figure 69 gives AM-PM conversions for NE800, NE371, and NE868 series. This data is particularly effective when designing a PCM transmitter. Figure 70 gives the standard characteristics for the third order intermodulation of NE800898-7H and NE868898-6.

This brief report explains current GaAs FET technology. Improvement of device characteristics is a major goal for both applied technology and research in electronics. GaAs FET reliability has already been confirmed and there is little doubt that FETs will eventually be used at frequencies of 40 GHz and higher.

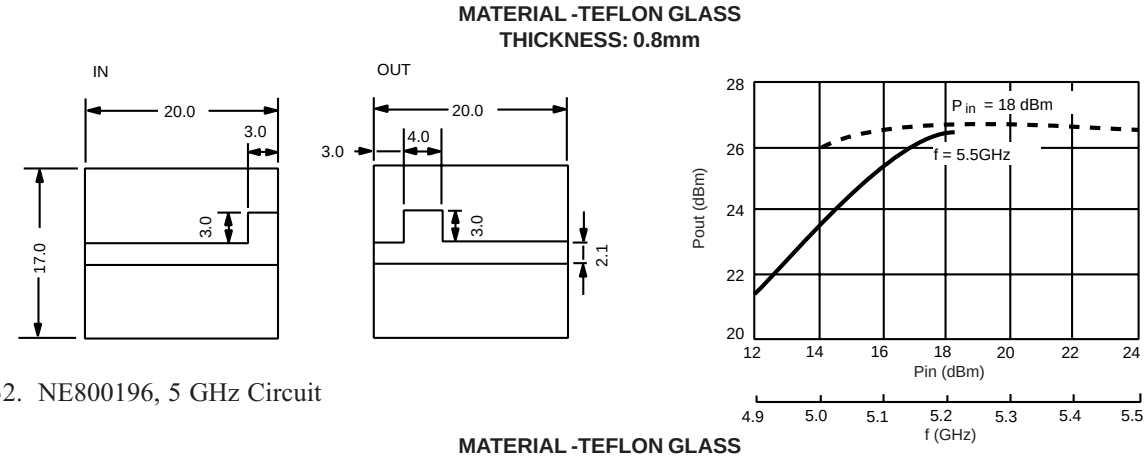


Figure 32. NE800196, 5 GHz Circuit

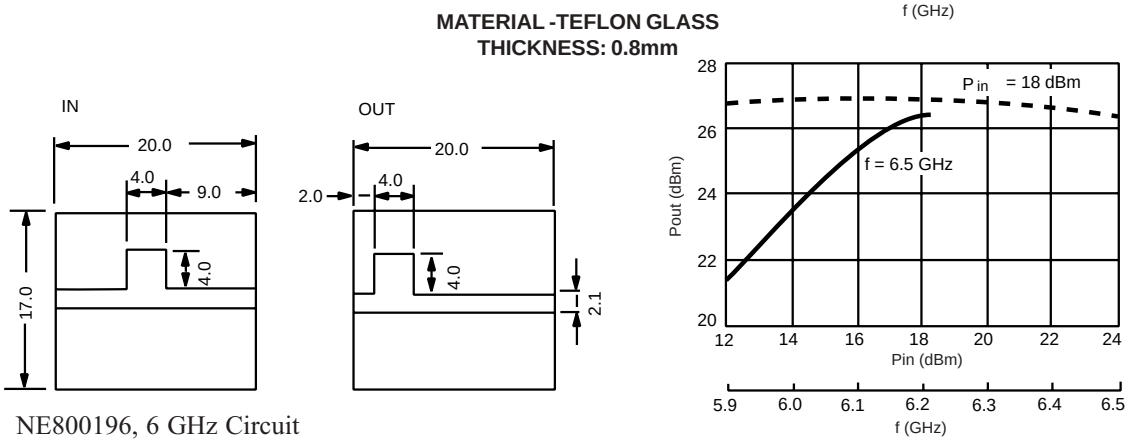


Figure 33. NE800196, 6 GHz Circuit

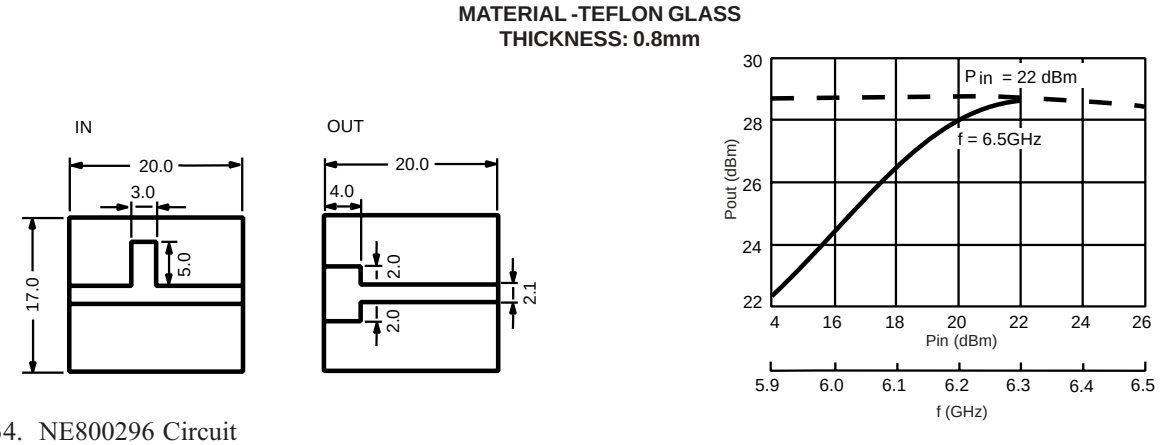


Figure 34. NE800296 Circuit

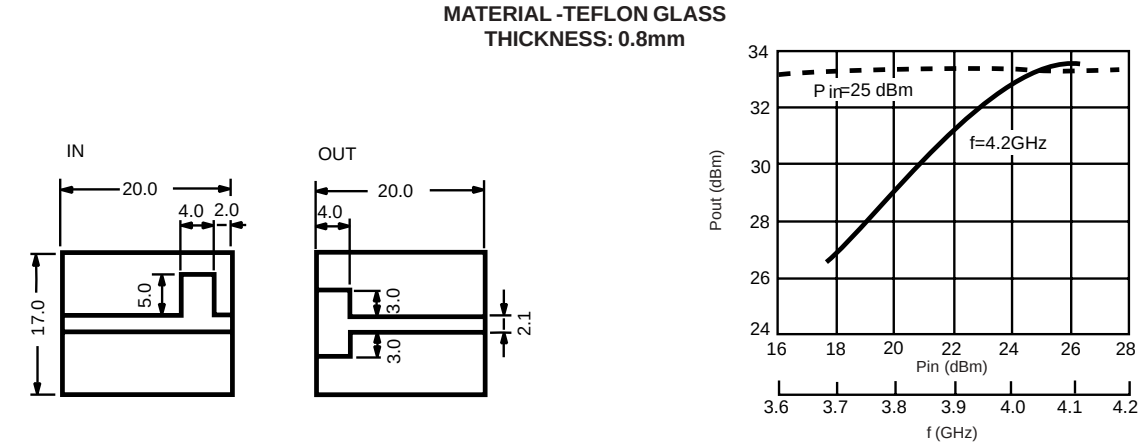


Figure 35. NE800495-4 Circuit

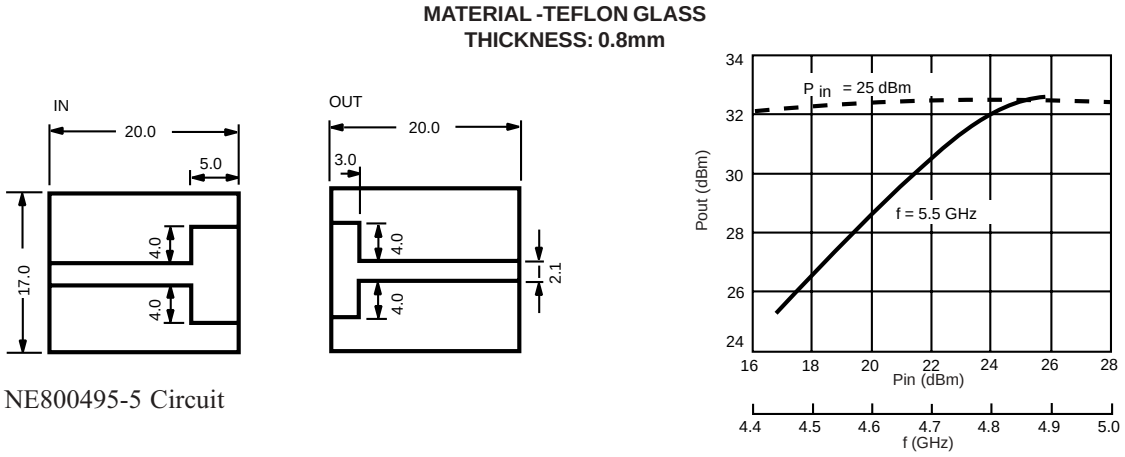


Figure 36. NE800495-5 Circuit

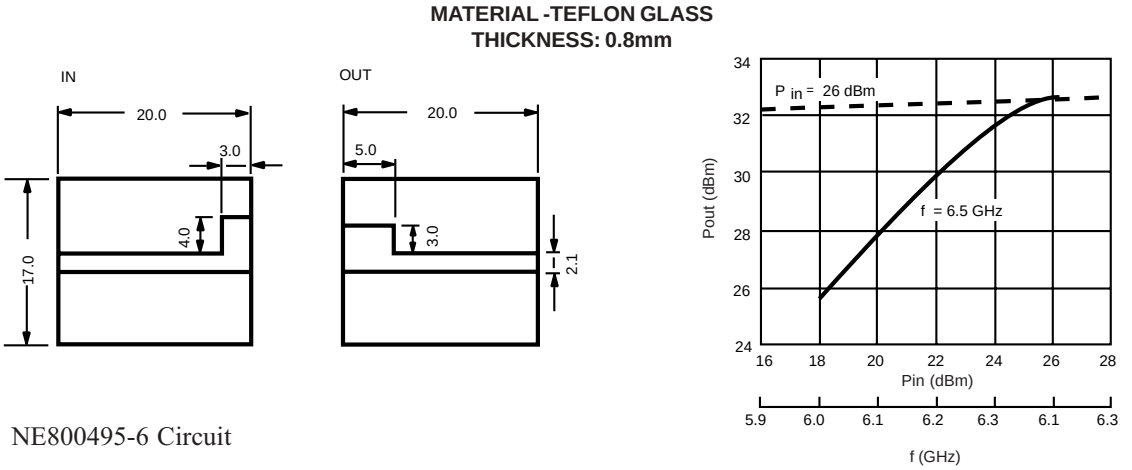


Figure 37. NE800495-6 Circuit

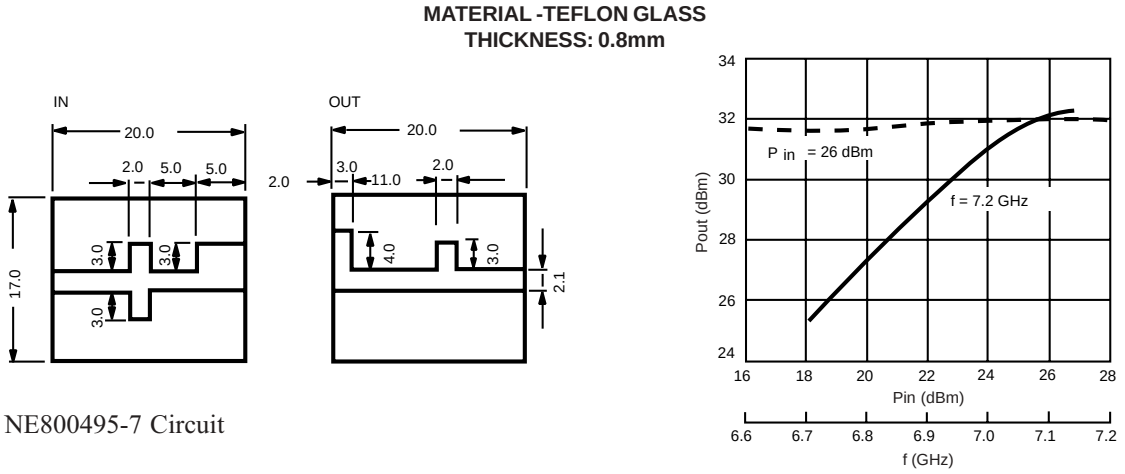


Figure 38. NE800495-7 Circuit

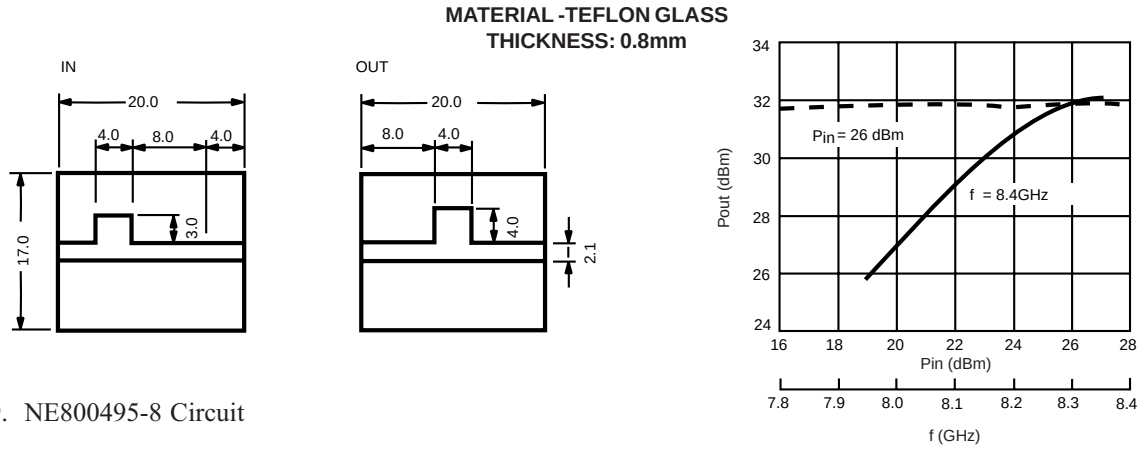


Figure 39. NE800495-8 Circuit

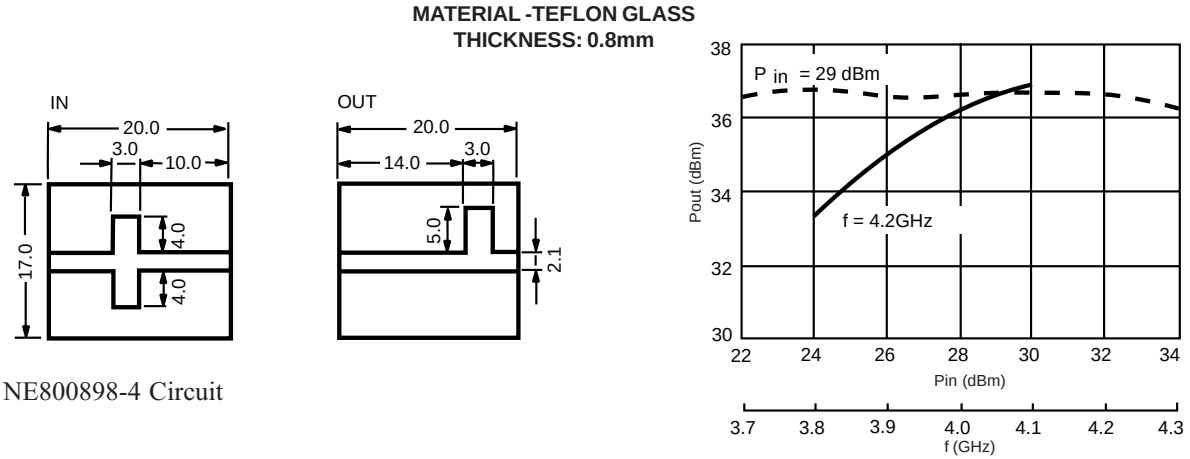


Figure 40. NE800898-4 Circuit

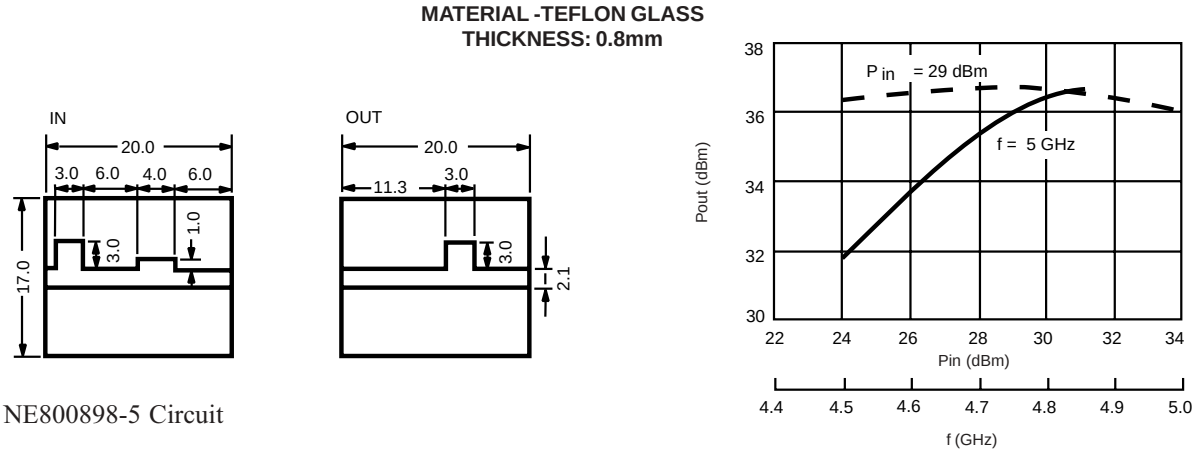


Figure 41. NE800898-5 Circuit

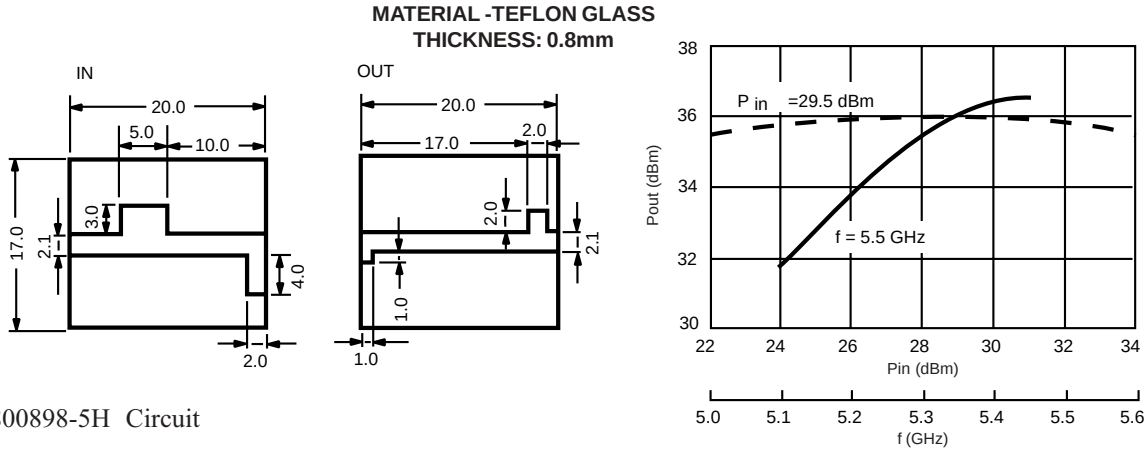


Figure 42. NE800898-5H Circuit

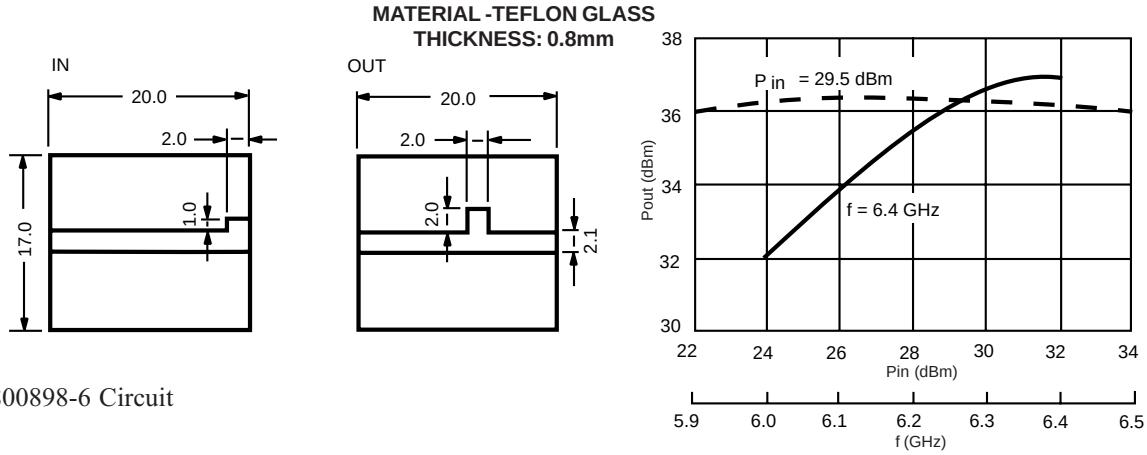
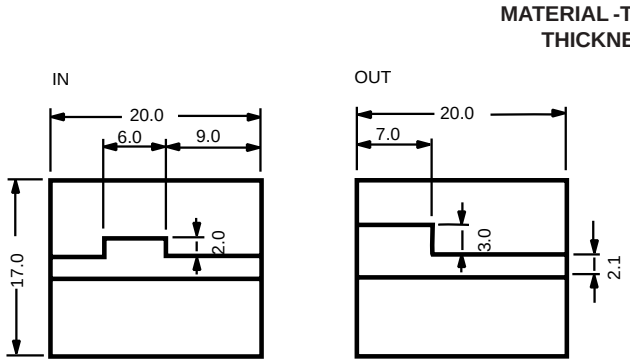


Figure 43. NE800898-6 Circuit



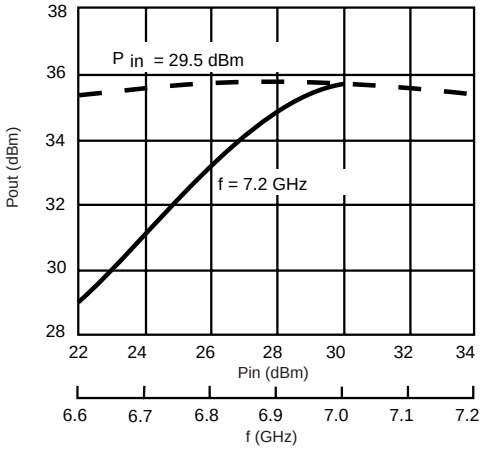
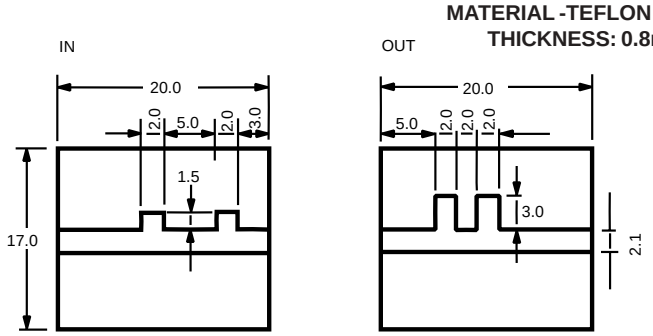


Figure 44. NE800898-7 Circuit



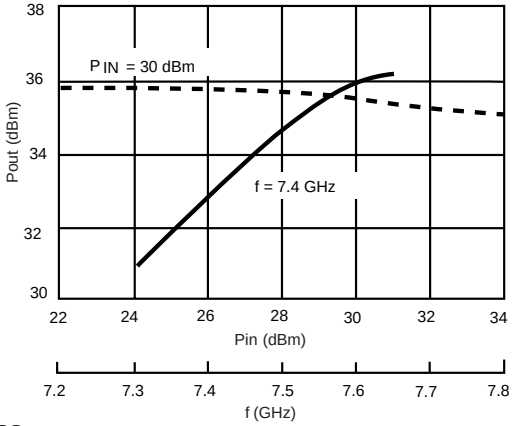
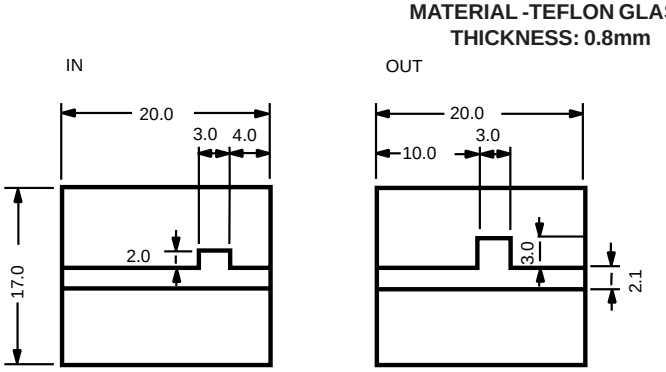


Figure 45. NE800898-7H Circuit



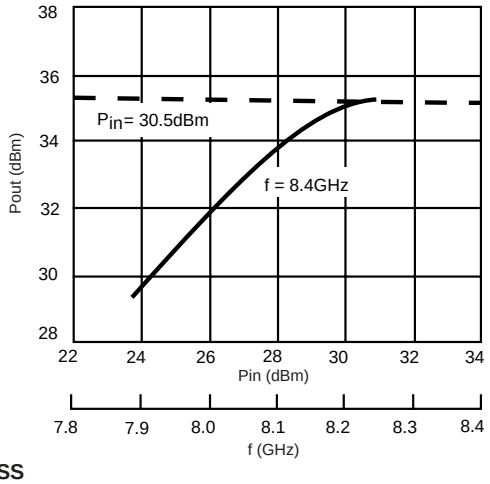
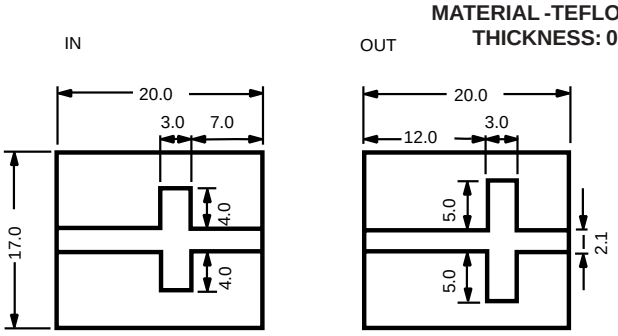


Figure 46. NE800898-8 Circuit



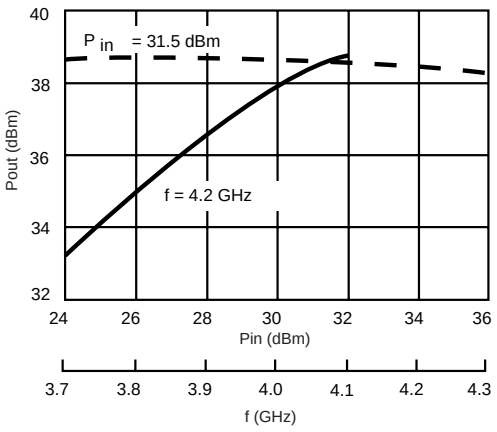


Figure 47. NE371698-4 Circuit

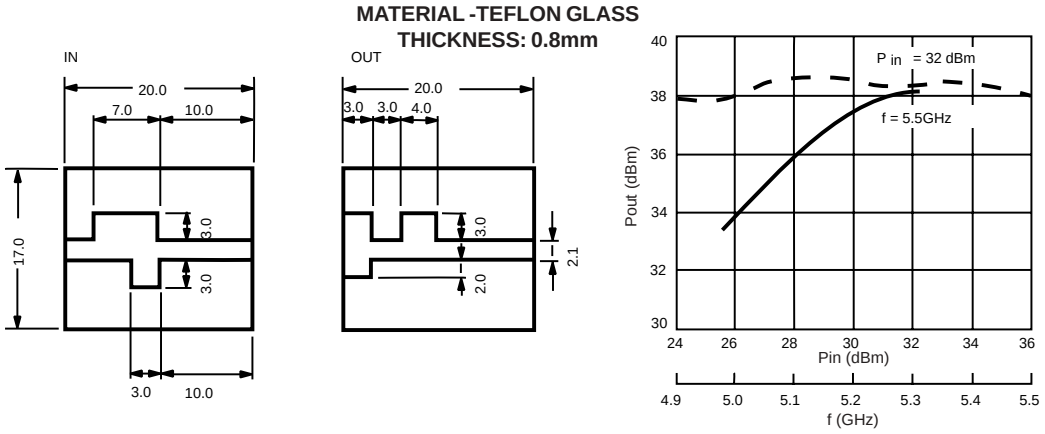


Figure 48. NE371698-5H Circuit

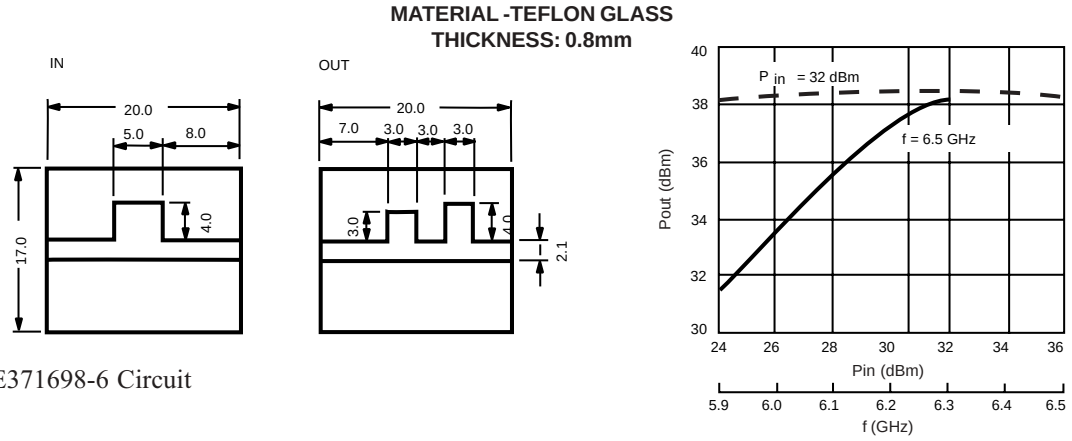


Figure 49. NE371698-6 Circuit

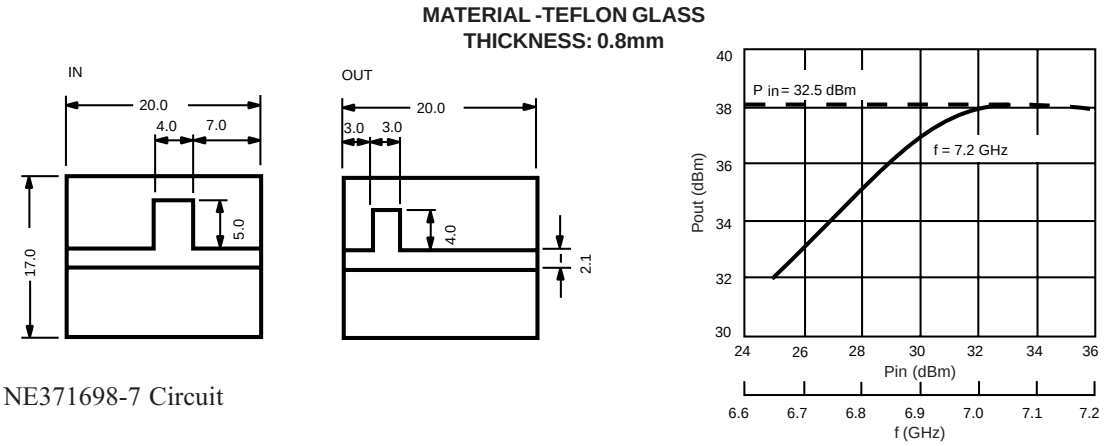


Figure 50. NE371698-7 Circuit

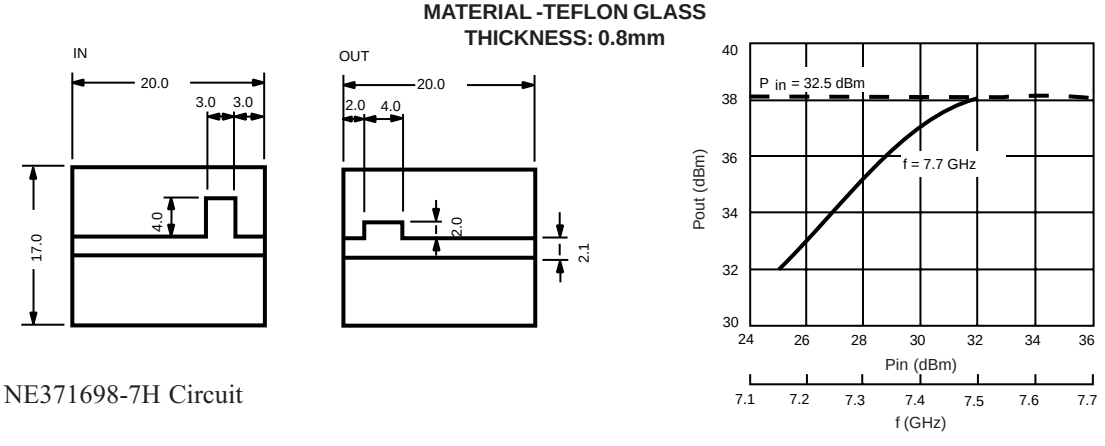


Figure 51. NE371698-7H Circuit

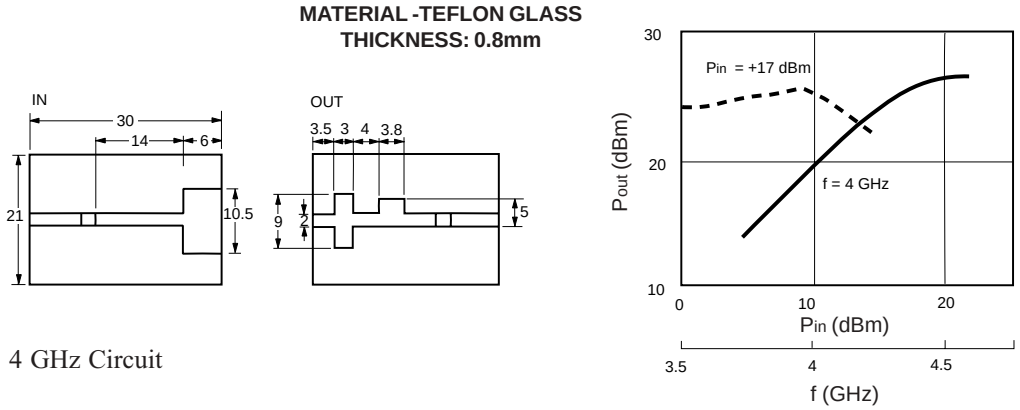


Figure 52. NE868196, 4 GHz Circuit

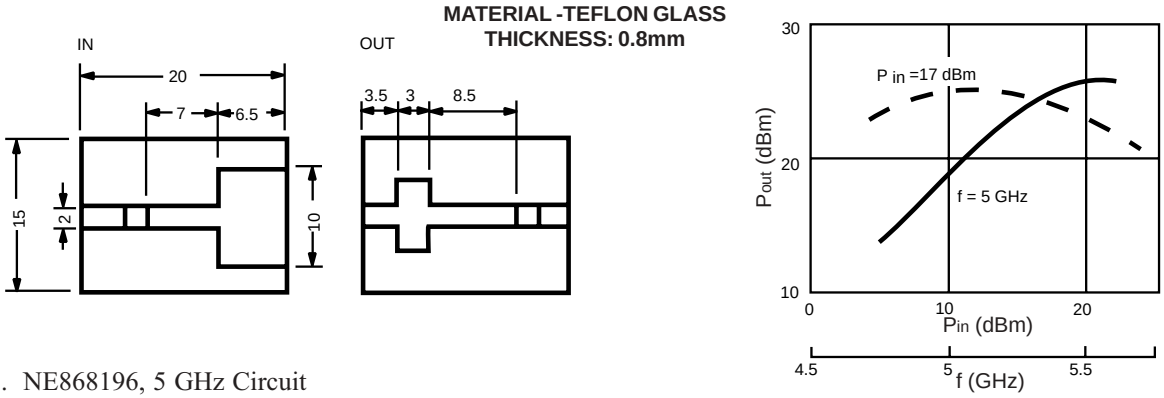


Figure 53. NE868196, 5 GHz Circuit

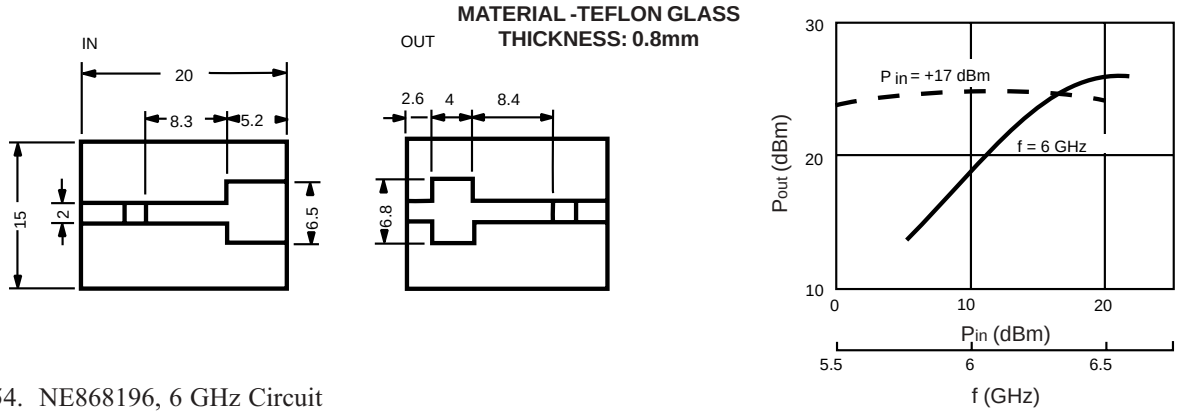


Figure 54. NE868196, 6 GHz Circuit

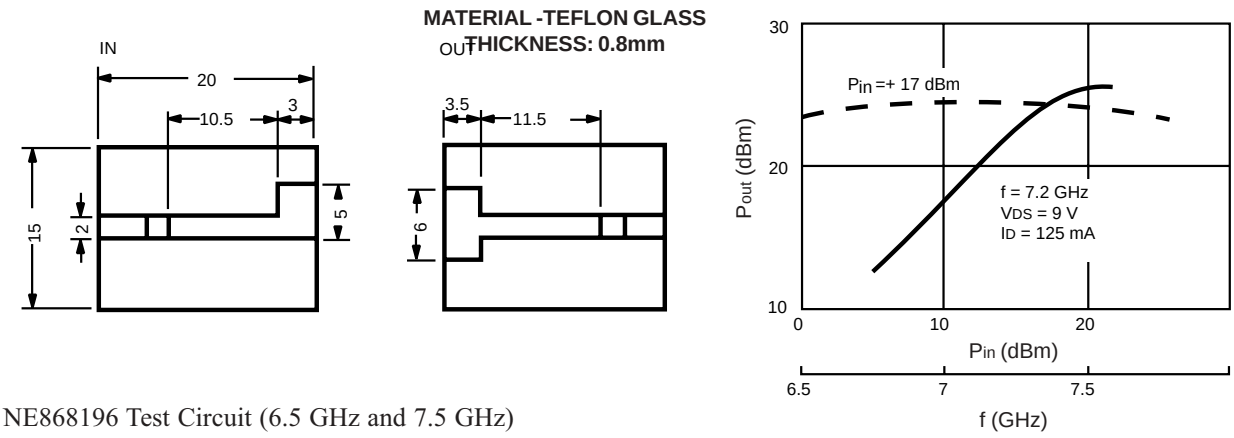


Figure 55. NE868196 Test Circuit (6.5 GHz and 7.5 GHz)

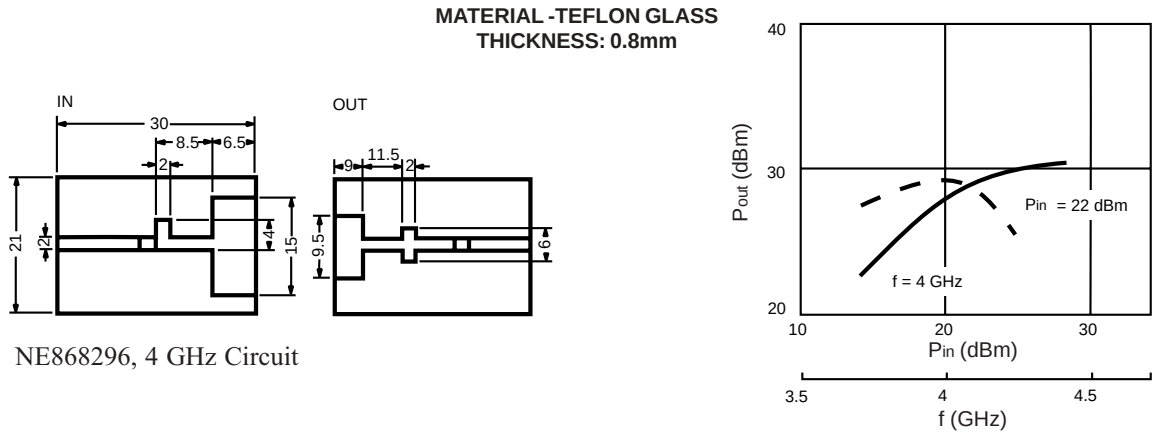


Figure 56. NE868296, 4 GHz Circuit

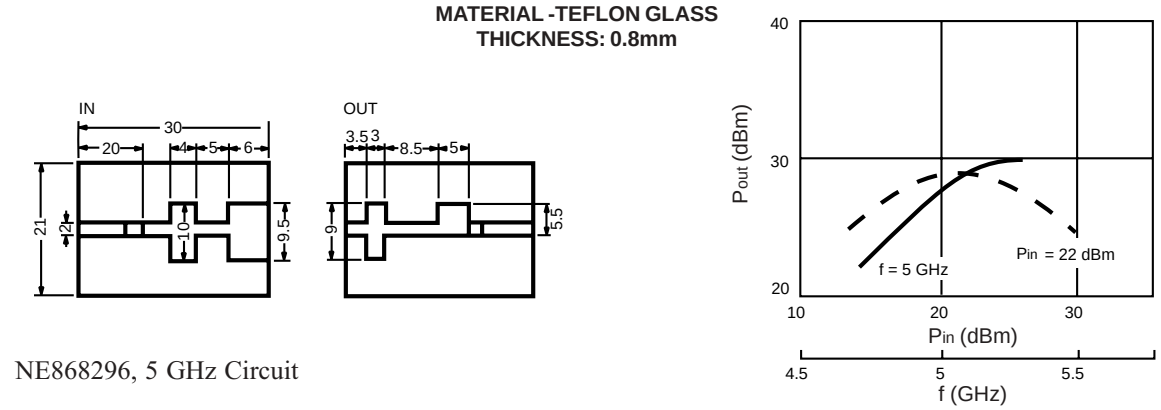


Figure 57. NE868296, 5 GHz Circuit

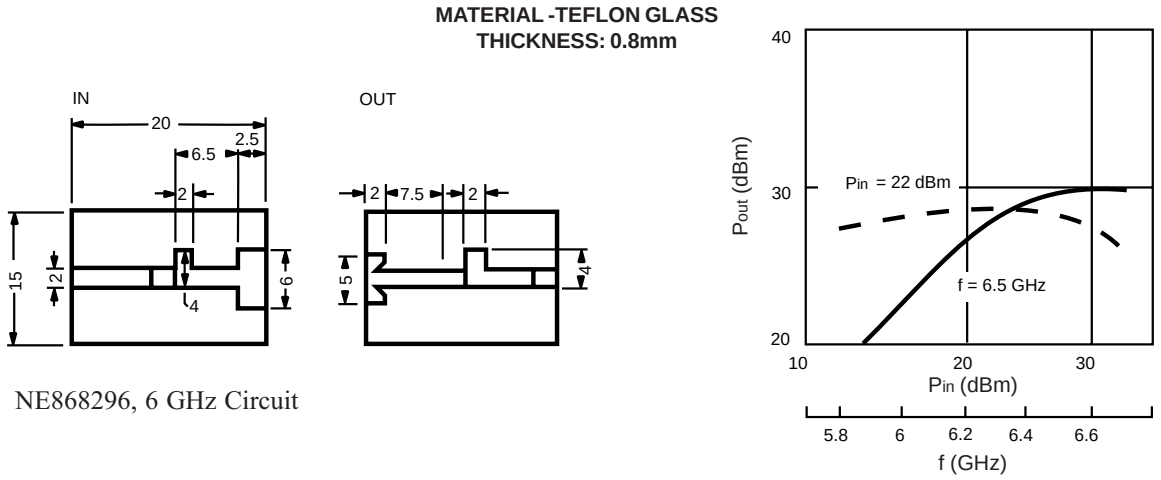


Figure 58. NE868296, 6 GHz Circuit

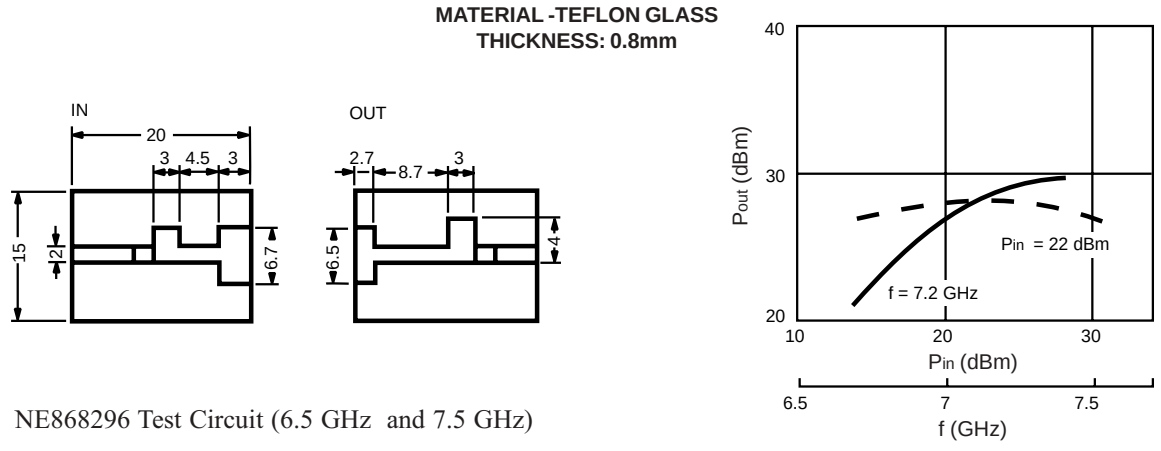


Figure 59. NE868296 Test Circuit (6.5 GHz and 7.5 GHz)

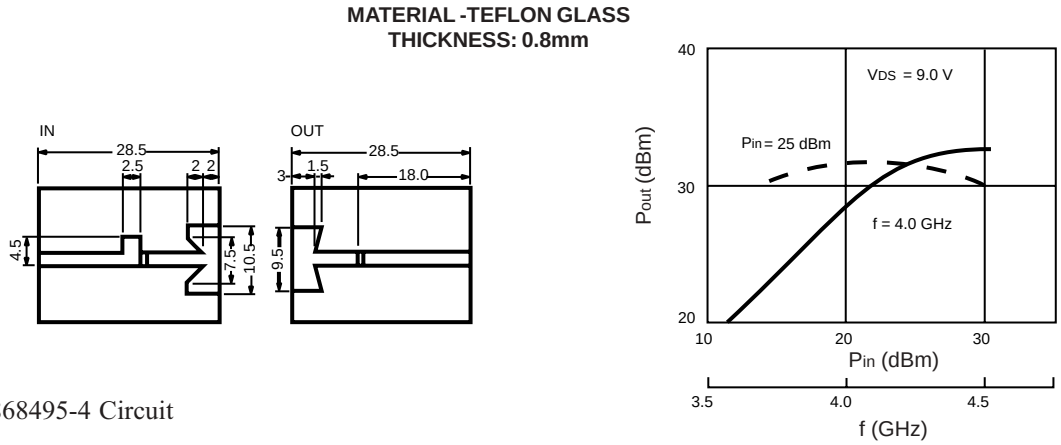


Figure 60. NE868495-4 Circuit

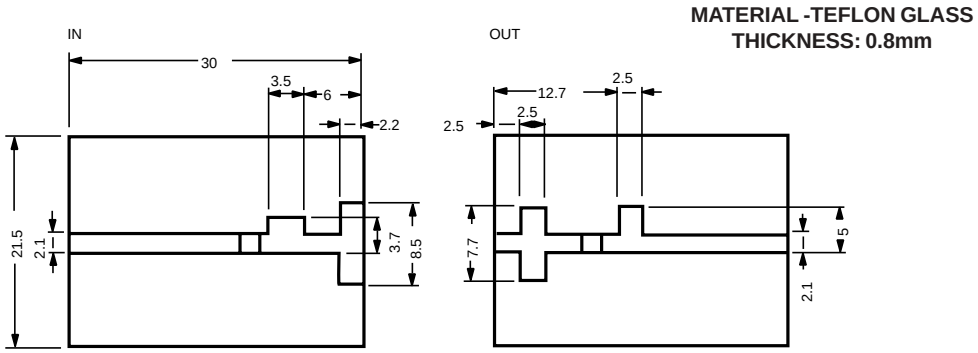


Figure 61. NE868495-5 Circuit

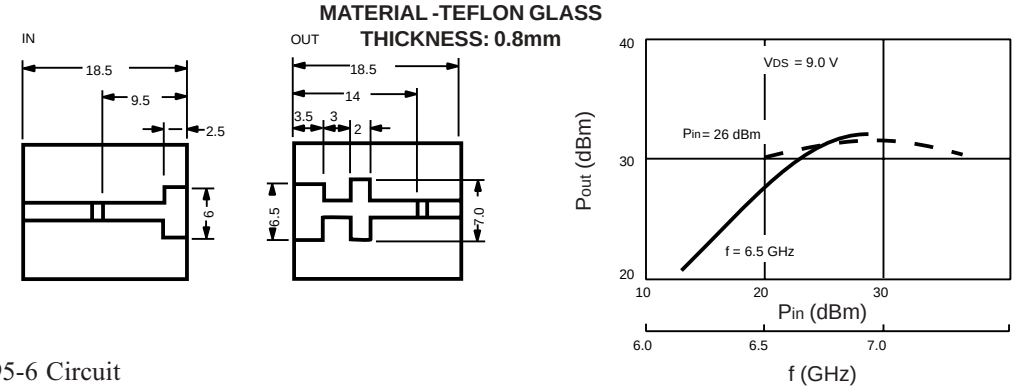


Figure 62. NE868495-6 Circuit

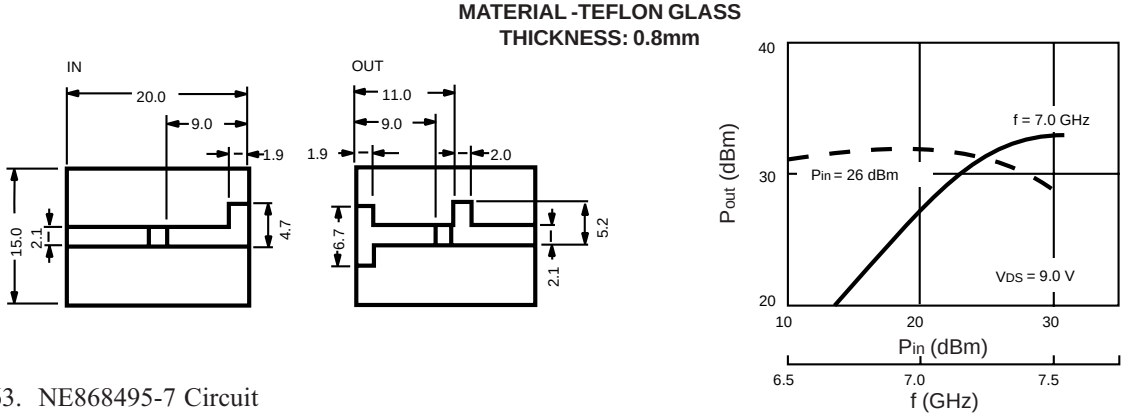


Figure 63. NE868495-7 Circuit

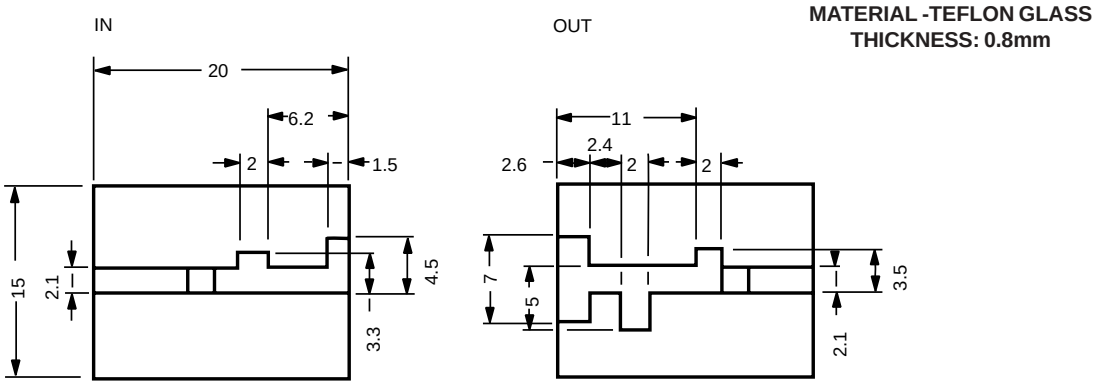


Figure 64. NE868495-8 Circuit

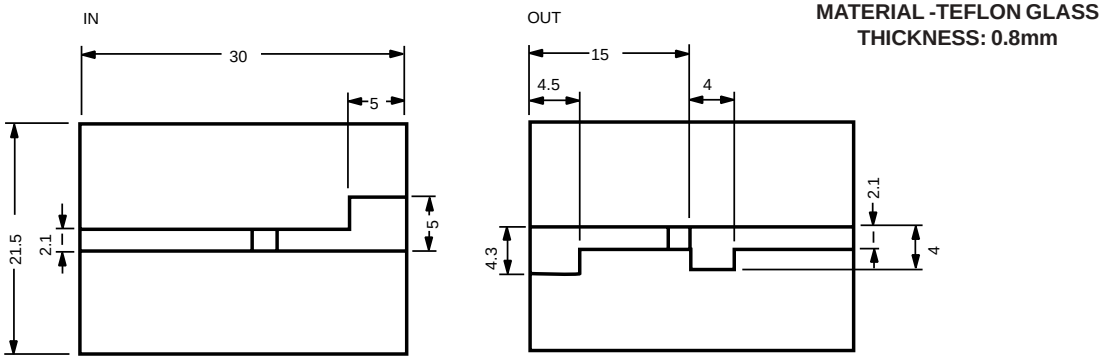


Figure 65. NE868898-5 Circuit

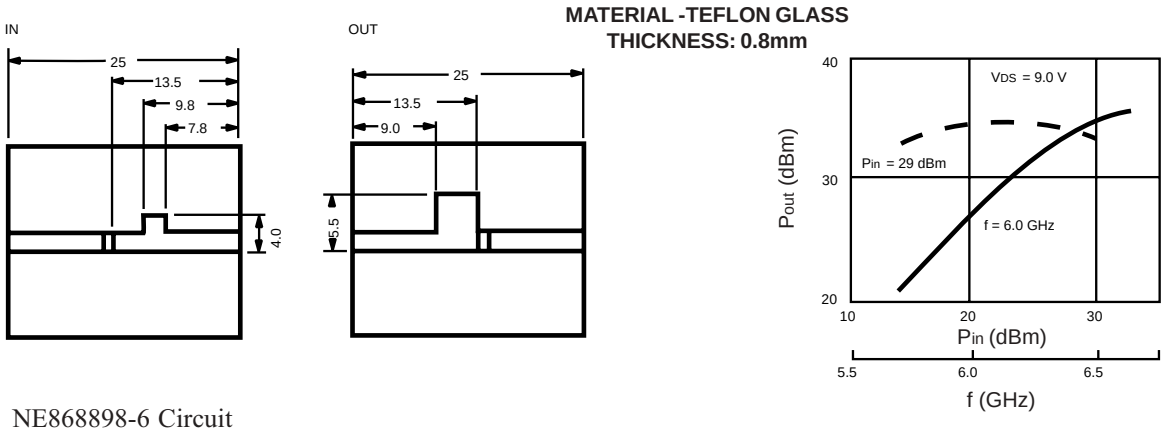


Figure 66. NE868898-6 Circuit

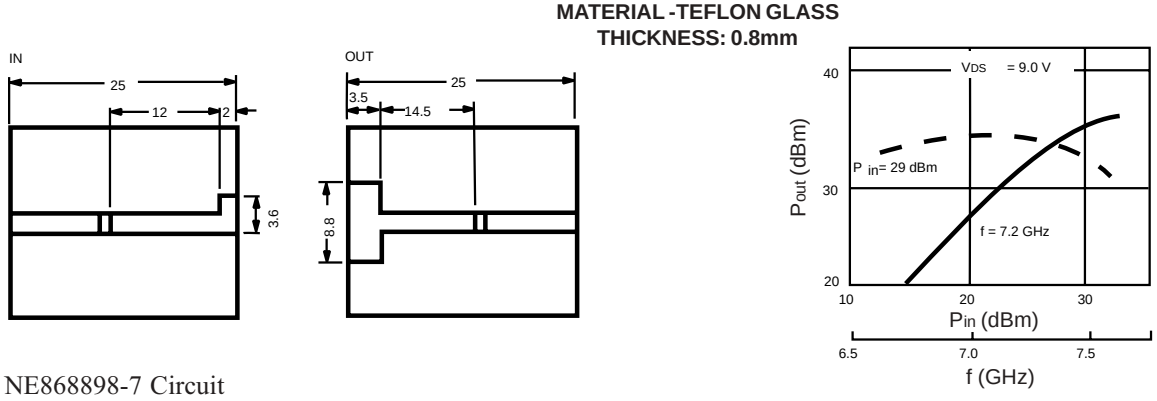


Figure 67. NE868898-7 Circuit

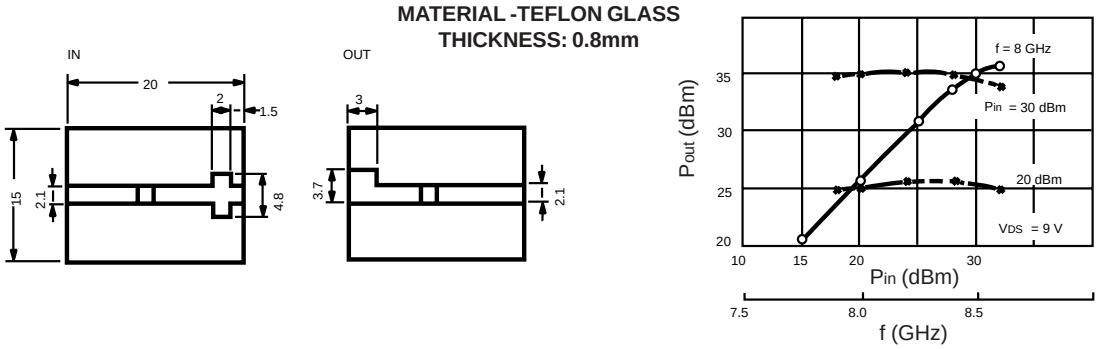


Figure 68. NE868898-8 Circuit

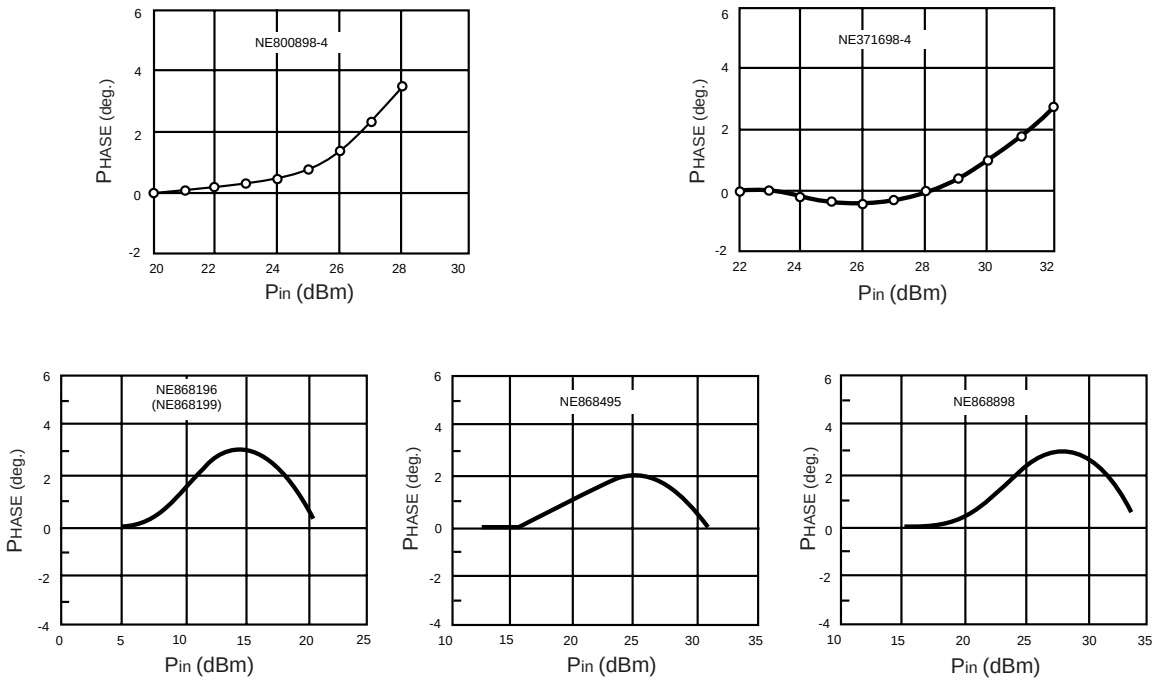


Figure 69. AM-PM Conversion for the NE800, NE371 and NE868 Series

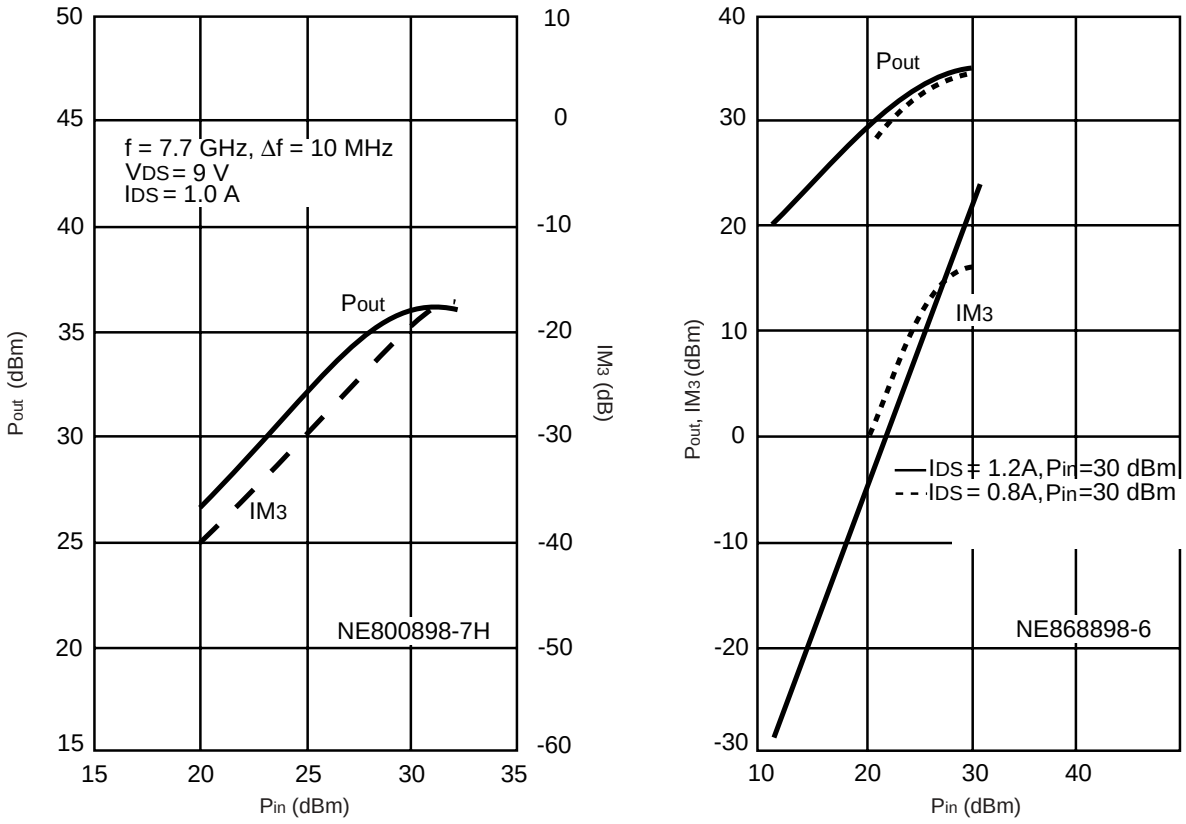


Figure 70. Third Order Intermodulation Distortions for the NE800898-7H and NE868898-6

References

[1] Masuo Fukuda, et. al., "Low Noise GaAs FET Ampliliers," MW77-21.

[2] Charles A Liechti, et. al., MTT-22, No. 5, May 1974

[3] Herman Sfatz, et. al., ED-21, No. 9, Sept. 1974.

[4] P. Bura, Electronics Letters, Vol. 10, No. 10, p. 181-,16th, May 1974.

[5] L. Nevin, et. al., "L-Band GaAs FET Amp.," Microwave Journal, Apr. 1979.

[6] Eric Ulrich, "Use Negative Feedback to Slash Wideband VSWR," Microwaves, Oct. 1978.

[7] K. Honjo, et. al., "Broadband Internal Matching of Microwave Power GaAs MES FETs.," IE3, Trans, Mit. Jan. 1979.

[8] Y. Takayama, "A New Load-Pull Characterization Method for Microwave Power Transistors," 1976 MTT-S, Digest, p. 218-220, June 1976.

California Eastern Laboratories

Exclusive Agents for NEC RF, Microwave and Optoelectronic semiconductor products in the U.S. and Canada

4590 Patrick Henry Drive, Santa Clara, CA 95054-1817
Telephone 408-988-3500 • FAX 408-988-0279 •Telex 34/6393
Internet: http:/WWW.CEL.COM

Information and data presented here is subject to change without notice. California Eastern Laboratories assumes no responsibility for the use of any circuits described herein and makes no representations or warranties, expressed or implied, that such circuits are free from patent infingement.

© California Eastern Laboratories 01/23/2003